M.E. Degree

in

VLSI DESIGN

CURRICULUM & SYLLABUS (CBCS)

(For students admitted from the Academic Year 2025-2026)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

St. XAVIER'S CATHOLIC COLLEGE OF ENGINEERING

CHUNKANKADAI, NAGERCOIL – 629 003.

KANYAKUMARI DISTRICT, TAMIL NADU, INDIA

St. XAVIER'S CATHOLIC COLLEGE OF ENGINEERING

Chunkankadai, Nagercoil – 629 003

AUTONOMOUS COLLEGE AFFILIATED TO ANNA UNIVERSITY

ACADEMIC REGULATIONS 2022

M.E. VLSI DESIGN CURRICULUM

CHOICE BASED CREDIT SYSTEM

Inconsonance to the vision of our College,

An engineering graduate we form would be a person with optimal human development, i.e. physical, mental, emotional, social and spiritual spheres of personality.

He/she would be also a person mature in relationships, especially knowing how to treat everyonewith respect, including persons of complementary gender with equality and gender sensitivity guidedby clear and pro-social values.

He would be patriotic and would hold the Indian Constitution and all the precepts it outlays close to his heart and would have a secular spirit committed to safeguard and cherish the multi-cultural, multi- religious and multi-linguistic ethos of Indian Society.

Academically, he/she would be a graduate with a strong engineering foundation with proficient technical knowledge and skills. He would have enough exposure and experience into the ethos of relevant industry and be industry ready to construct a successful career for himself and for the benefit of the society.

He would have been well trained in research methodology and would have established himself as a researcher having taken up many research projects, with sound ethical standards and social relevance. He would be a person with a passion for technical innovations committed to lifelong learning and research.

He would be well prepared and confident to develop ingenuous solutions to the problems people face as an individual and as a team and work for the emancipation of our society with leadership and courage.

ME (VLSI Design) is a PG course in Electronics and Communication Engineering that is made to acquire in-depth knowledge of Analog and Digital IC designs, System On Chip designs which can find it's application in the field of communication, signal processing and networking, computer design etc. including wider and global perspective. The course is for 2 years which is then divided into 4 semesters.

This course offers a comprehensive, in-depth study on analog and digital systems for making chips using latest technologies, low power design techniques for minimizing power consumption, VLSI testing methods for improving the yield.

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I. PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

I.	Apply technical knowledge and skills to have successful career in industry, government and academia as VLSI engineers.
II.	Pursue multidisciplinary scientific research in VLSI and related areas for the benefits of society.
III.	Make use of various state-of art systems and cutting-edge technologies to solve various complex engineering problems.
IV.	Inculcate leadership skills, team work, effective communication and lifelong learning to the success of their organization and nation.
V.	Practice ethics and exhibit commitment in profession to empower / enable rural communication infrastructure.

II. PROGRAMME OUTCOMES (POs)

PO#	Programme Outcomes
1	Independently carry out research/investigation and development work to solve practical problems.
2	Write and present substantial technical report/document.
3	Demonstrate a degree of mastery over the techniques in the area of analog and digital VLSI system design.
4	Analyze and design the subsystems in RF, signal processing, modern communication systems and networks.
5	Solve problems in analog and digital system design using advanced hardware and software tools.
6	Interact effectively with the technical experts in industry and society.

PEO's – PO's MAPPING:

PEOPROGRAMME EDUCATIONAL OBJECTIVES	PROGRAMME OUTCOMES					
	1	**2**	**3**	**4**	**5**	**6**
I.	**2**	**1**	**2**	**3**	**3**	**2**
II.	**2**	**1**	**2**	**3**	**3**	**2**
III.	**2**	**1**	**2**	**3**	**3**	**2**
IV.	**2**	**1**	**2**	**-**	**-**	**-**
V.	**1**	**1**	**2**	**-**	**-**	**2**

PROGRAMME ARTICULATION MATRIX

Year	Semester	Course name	PO					
			1	**2**	**3**	**4**	**5**	**6**
I	I	Graph Theory and Optimization Techniques	2	-	1	1	-	-
		Analog IC Design	1	-	2	2	1	-
		Semiconductor Devices and Modeling	2	-	1	1	2	-
		Advanced Digital System Design	1	-	1	1	1	-
		Analog IC Design Laboratory	2	-	2	3	2	-
		Technical Seminar	3	3	2	-	-	3
		Research Methodology	-	2	3	-	-	2
	II	Digital CMOS VLSI Design	2	-	2	-	2	1
		Design for Verification using UVM	1	-	1	1	2	1
		ASIC Design	2	-	2	2	1	1

		Low Power VLSI Design	2	-	2	2	2	-
		FPGA Laboratory	2	-	2	2	2	-
		Research Tool Laboratory	2	2	1	-	-	-
II	III	Project Work I	3	3	3	3	3	3
	IV	Project Work II	3	3	3	3	3	3

M.E. VLSI DESIGN CURRICULUM

SEMESTER I

SL. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY COURSES								
1	MA22109	Graph Theory and Optimization Techniques	FC	3	1	0	4	4
2	VL22101	Analog IC Design	PCC	3	0	0	3	3
3	VL22102	Semiconductor Devices and Modeling	PCC	3	0	0	3	3
THEORY COURSES WITH PRACTICAL COMPONENT								
4	VL22103	Advanced Digital System Design	PCC	3	0	2	5	4
PRACTICAL COURSES								
5	VL22104	Analog IC Design Laboratory	PCC	0	0	4	4	2
EMPLOYABILITY ENHANCEMENT COURSES								
6	VL22105	Technical Seminar	EEC	0	0	2	2	1
7	RM22101	Research Methodology	RMC	2	0	0	2	2
MANDATORY COURSES								
8		Audit Course I	AC	2	0	0	2	0
TOTAL				**16**	**1**	**8**	**25**	**19**

SEMESTER II

SL. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY COURSES								
1	VL22201	Digital CMOS VLSI Design	PCC	3	0	0	3	3
2		Professional Elective I	PEC	3	0	0	3	3
3		Professional Elective II	PEC	3	0	0	3	3
THEORY COURSES WITH PRACTICAL COMPONENT								
4	VL22202	Design for Verification using UVM	PCC	3	0	2	5	4
5	VL22203	ASIC Design	PCC	3	0	2	5	4

6	VL22204	Low Power VLSI Design	PCC	3	0	2	5	4
PRACTICAL COURSES								
7	VL22205	FPGA Laboratory	PCC	0	0	4	4	2
EMPLOYABILITY ENHANCEMENT COURSES								
8	RM22201	Research Tool Laboratory	RMC	0	0	4	4	2
MANDATORY COURSES								
9		Audit Course II	AC	2	0	0	2	0
TOTAL				**20**	**0**	**14**	**34**	**25**

SEMESTER III

SL. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY COURSES								
1		Professional Elective III	PEC	3	0	0	3	3
2		Open Elective	OEC	3	0	0	3	3
THEORY COURSES WITH PRACTICAL COMPONENT								
3		Professional Elective IV	PEC	3	0	2	5	4
EMPLOYABILITY ENHANCEMENT COURSES								
4	VL22301	Inplant / Industrial / Practical Training (4 weeks during summer vacation)	EEC	0	0	4	4	2
5	VL22302	Project Work I	EEC	0	0	6	6	3
TOTAL				**9**	**0**	**12**	**21**	**15**

SEMESTER IV

SL. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
EMPLOYABILITY ENHANCEMENT COURSES								
1	VL22401	Project Work II	EEC	0	0	24	24	12
TOTAL				**0**	**0**	**24**	**24**	**12**

TOTAL CREDITS: 71

PROFESSIONAL ELECTIVES

SEMESTER II, PROFESSIONAL ELECTIVES – I

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL22211	CMOS Fabrication Technology	PEC	3	0	0	3	3
2.	VL22212	Electromagnetic Interference and Compatibility	PEC	3	0	0	3	3
3.	VL22213	Advanced Wireless Sensor Networks	PEC	3	0	0	3	3

4.	VL22114	Hardware Software Co Design	PEC	3	0	0	3	3
5.	VL22215	Hardware Security	PEC	3	0	0	3	3
6.	VL22216	Pattern Recognition	PEC	3	0	0	3	3

SEMESTER II, PROFESSIONAL ELECTIVES – II

Sl. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL22221	Mixed Signal VLSI Design	PEC	3	0	0	3	3
2.	VL22222	VLSI for Wireless Communication	PEC	3	0	0	3	3
3.	VL22223	RF IC Design	PEC	3	0	0	3	3
4.	VL22224	Embedded Sysem Design	PEC	3	0	0	3	3
5.	VL22225	Power Management and Clock Distribution Circuits	PEC	3	0	0	3	3
6.	VL22226	Reconfigurable Architectures	PEC	3	0	0	3	3

SEMESTER III, PROFESSIONAL ELECTIVES – III

Sl. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL22311	VLSI Testing	PEC	3	0	0	3	3
2.	VL22312	Signal Integrity for High Speed Design	PEC	3	0	0	3	3
3.	VL22313	VLSI Signal Processing	PEC	3	0	0	3	3
4.	VL22314	CAD for VLSI Design	PEC	3	0	0	3	3
5.	VL22315	System On Chip	PEC	3	0	0	3	3
6.	VL22316	Nano Scale Devices	PEC	3	0	0	3	3

SEMESTER III, PROFESSIONAL ELECTIVES - IV

Sl. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL22321	Physical Design Automation	PEC	3	0	2	5	4
2.	VL22322	System Verilog	PEC	3	0	2	5	4
3.	VL22323	Digital Imaging and Video Processing	PEC	3	0	2	5	4
4.	MX22313	Deep Learning	PEC	3	0	2	5	4
5.	VL22324	PCB Design	PEC	3	0	2	5	4
6.	VL22325	Adaptive Signal Processing	PEC	3	0	2	5	4

AUDIT COURSES (AC)

SL. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS
			L	T	P	
1.	AC22101	English for Research Paper Writing	2	0	0	0
2.	AC22102	Constitution of India	2	0	0	0
3.	AC22201	Disaster Management	2	0	0	0
4.	AC22202	நற்றமிழ் இலக்கியம	2	0	0	0

SUMMARY

M.E. VLSI Design						
S.No	Subject Area	Credits per Semester				Total Credits
		I	II	III	IV	
1	FC	4	-	-	-	**4**
2	PCC	12	17	-	-	**29**
3	PEC	-	6	7	-	**13**
4	OEC	-	-	3	-	**3**
5	EEC	1	2	5	12	**20**
6	RMC	2	-	-	-	**2**
7	Non-Credit AC	0	0	-	-	**0**
TOTAL		**19**	**25**	**15**	**12**	**71**

SEMESTER – I

MA22109	GRAPH THEORY AND OPTIMIZATION TECHNIQUES	L	T	P	C
		3	1	0	4

COURSE OBJECTIVES:

- To introduce graph as mathematical model to solve connectivity related problems.
- To introduce fundamental graph algorithms
- To familiarize the students with the formulation and construction of a mathematical model for a linear programming problem in a real-life situation
- To understand, develop and solve mathematical model of Transportation and assignment problems
- To understand the applications of simulation modeling in engineering problems

UNIT I	GRAPHS	12

Graphs and graph models – Graph terminology and special types of graphs – Matrix representation of graphs and graph isomorphism- Connectivity (Definitions and examples only)– Euler and Hamilton paths (Definitions and examples only).

UNIT II	GRAPH ALGORITHM	12

Graph Algorithms – Directed graphs – Some basic algorithms – Shortest path algorithms – Depth – First search on a graph – Theoretic algorithms – Performance of graph theoretic algorithm.

UNIT III	LINEAR PROGRAMMING	12

Formulation of liner programming problem - Graphical method of solution –Canonical and standard form of liner programming problem - Some important definitions - Simplex Method – Two phase method

UNIT IV	TRANSPORTATION AND ASSIGNMENT MODELS	12

Definition of the transportation model - Formulation - Basic feasible solution: North- West corner rule - least cost method- Vogel's approximation method - Definition of the assignment Model - Mathematical formulation of assignment models – Hungarian method for solution of the assignment problem

UNIT V	SIMULATION MODELLING	12

Monte Carlo Simulation – Types of Simulation – Elements of Discrete Event Simulation – Generation

of Random Numbers.	
TOTAL: 60 PERIODS	
COURSE OUTCOMES:	
Upon completion of the course, the students will be able to	
CO1	Apply graph as mathematical model to solve connectivity related problems.
CO2	Apply fundamental graph algorithms to solve certain optimization problems
CO3	Formulate and construct mathematical models for linear programming problems
CO4	Apply linear programming problem in transportation and assignment models to find initial and optimal solution
CO5	Apply simulation modeling techniques to problems drawn from industry management and other engineering fields
REFERENCES:	
1.	Taha H.A, "Operation Research: An Introduction", Ninth Edition, Pearson Education, New Delhi, 2010.
2.	Gupta P. K, and Hira D.S., "Operation Research", Revise Edition, S. Chand and Company Ltd., 2012.
3.	Sharma J.K., "Operation Research", Third Edition, Macmillan Publishers India Ltd.,2009.
4.	Douglas B. West, "Introduction to Graph Theory", Pearson Education, New Delhi,2015.
5.	Balakrishna R., Ranganathan. K., "A text book of Graph Theory", Springer Science and Business Media, New Delhi, 2012.
6.	Narasingh Deo, "Graph Theory with Applications to Engineering and Computer Science", Prentice Hall India,1997.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	2	-	1	1	-	-
CO2	2	-	1	1	-	-
CO3	2	-	1	1	-	-
CO4	2	-	1	1	-	-
CO5	2	-	1	1	-	-
CO	2	-	1	1	-	-

VL22101	**ANALOG IC DESIGN**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**
COURSE OBJECTIVES:					
• To learn the basics of single stage analog CMOS amplifiers					
• To gain knowledge in noise characteristics of amplifiers					
• To study the performance parameters of amplifiers and compensation techniques					
• To design an analog amplifier with band gap reference					
UNIT I	**SINGLE STAGE AMPLIFIERS**				**9**
Basic MOS physics and equivalent circuits and models - CS, CG and Source Follower- differential amplifier with active load- Cascode and Folded Cascode configurations with active load- design of Differential and Cascode Amplifiers- to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, high gain amplifier structures.					
UNIT II	**HIGH FREQUENCY AND NOISE CHARACTERISTICS OF AMPLIFIERS**				**9**
Current mirrors, cascode stages for current mirrors, current mirror loads for differential pairs. Miller effect, association of poles with nodes, frequency response of CS, CG and source follower, cascode and differential pair stages, Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers.					
UNIT III	**FEEDBACK AND OPERATIONAL AMPLIFIERS**				**9**
Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, Single stage Op Amps, two-stage Op Amps, input range limitations,					

gain boosting, slew rate, power supply rejection, noise in Op Amps.		
UNIT IV	**STABILITY AND FREQUENCY COMPENSATION**	**9**
General considerations, Multiple systems, Phase Margin, Frequency Compensation, Compensation of two stage Op Amps, Slewing in two stage Op Amps, Other compensation techniques.		
UNIT V	**BAND GAP REFERENCE**	**9**
Supply independent biasing, temperature-independent references, negative-TC voltage, positive TC voltage, Bandgap reference, PTAT generation, curvature correction, Design of BGR under low voltage conditions.		
		TOTAL: 45 PERIODS

COURSE OUTCOMES:	
Upon completion of the course, the students will be able to	
CO1	Explain the basics of single stage analog CMOS amplifiers.
CO2	Summarize the noise characteristics and frequency response of single stage amplifiers.
CO3	Explain the performance parameters of feedback and differential amplifiers.
CO4	Comprehend the compensation techniques in Op Amps.
CO5	Design band gap reference circuits.

REFERENCES:	
1.	Behzad Razavi, Design of Analog CMOS Integrated Circuit, McGraw Hill Education, 2017, Second Edition.
2.	Paul J. Hurst, Paul R. Gray, Robert G Meyer and Stephen H. Lewis, Analysis and Design of Analog Integrated Circuits, Wiley, 2024, Sixth Edition.
3.	Paul G. A. Jespers, Boris Murmann, "Systematic Design of Analog CMOS Circuits", Cambridge University press, 2017.
4.	Johan Huijsing, Rudy J. Van Der Plassche, Willy M.C. Sansen , "Analog Circuit Design: Operational Amplifiers, Analog to Digital Convertors, Analog Computer Aided Design", Springer US , 2013. Third Edition.
5.	David Johns, Tony Chan Carusone and Kenneth Martin, Analog Integrated Circuit Design, Wiley, 2011, Second Edition.
6.	Phillip E.Allen, Douglas R.Holberg, "CMOS Analog Circuit Design", Second edition, Oxford University Press, 2011.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	**Programme Outcomes**					
	1	**2**	**3**	**4**	**5**	**6**
CO1	1	-	2	2	1	-
CO2	1	-	2	2	1	-
CO3	1	-	2	2	1	-
CO4	1	-	2	2	1	-
CO5	1	-	2	2	1	-
CO	1	-	2	2	1	-

VL22102	**SEMICONDUCTOR DEVICES AND MODELING**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:		
• To develop a strong foundation in semiconductor theory, devices, and their practical applications.		
• To gain comprehensive knowledge of semiconductor device modeling and its relevance to the design of electronic systems.		
• To understand various aspects of semiconductor device modeling essential for advanced electronic design and analysis.		
UNIT I	**MOS CAPACITORS**	**9**

Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in an MOS Structure, Polysilicon-Gate Work Function and Depletion Effects, Charge in Silicon Dioxide and at the Silicon–Oxide Interface, High-Field Effects: Impact Ionization and Avalanche Breakdown, Band-to-Band Tunneling, Tunneling into and through Silicon Dioxide, Injection of Hot Carriers from Silicon into Silicon Dioxide.		
UNIT II	**MOSFET DEVICES**	**9**
Long-Channel MOSFETs: Drain-Current Model, MOSFET I–V Characteristics, Subthreshold Characteristics, MOSFET Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, Short-Channel MOSFETs, Short-Channel Effect, Velocity Saturation, Channel Length Modulation, MOSFET Breakdown.		
UNIT III	**CMOS DEVICE DESIGN**	**9**
MOSFET Scaling: Constant-Field Scaling, Constant-Voltage Scaling, Nonscaling Effects, Threshold Voltage, Threshold-Voltage Requirement, Channel Profile Design, Nonuniform Doping, Quantum Effect on Threshold Voltage, MOSFET Channel Length: Various Definitions of Channel Length, Extraction of the Effective Channel Length, Extraction of Channel Length by C–V Measurements.		
UNIT IV	**BIPOLAR DEVICES**	**9**
Modifying the Simple Diode Theory for Describing Bipolar Transistors, Ideal Current–Voltage Characteristics: Current density equation, Collector current, Base current, Characteristics of a Typical n–p–n Transistor: Effect of Emitter and Base Series Resistances, Effect of Base–Collector Voltage on Collector Current, Collector Current Falloff at High Currents, Bipolar Device Models for Circuit and Time-Dependent Analyses: Basic dc Model, Basic ac Model, Small-Signal Equivalent-Circuit Model, Emitter Diffusion Capacitance.		
UNIT V	**MATHEMATICAL TECHNIQUES FOR DEVICE SIMULATIONS**	**9**
Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations.		
		TOTAL: 45 PERIODS
COURSE OUTCOMES:		
Upon completion of the course, the students will be able to		
CO1	Understand the electrostatics of MOS capacitors.	
CO2	Illustrate the operation and characteristics of long-channel and short-channel MOSFETs.	
CO3	Explain CMOS device design principles. Summarize the device level characteristics of BJT transistors.	
CO4	Describe the functioning and modeling of bipolar junction transistors.	
CO5	Interpret the key mathematical models and equations used in semiconductor device simulations.	
REFERENCES:		
1.	Yuan Taur and Tak H. Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, Second Edition,2016.	
2.	Behzad Razavi," Fundamentals of Microelectronics", Wiley Student Edition, third edition Edition,2021.	
3.	Ansgar Jungel, "Transport Equations for Semiconductors", Springer, 2009	
4.	Selberherr, S., "Analysis and Simulation of Semiconductor Devices", Springer-Verlag., 1984	
5.	S.M. Sze, Kwok.K. NG, "Physics of Semiconductor devices", Third edition, Springer, 2021	
6.	A.B. Bhattacharyya "Compact MOSFET Models for VLSI Design", John Wiley & Sons	

	Ltd, 2009.
7.	J P Collinge, C A Collinge, “Physics of Semiconductor devices” Springer, 2002.
8.	Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly Wayne Wolf, “Device Modeling for Analog and RF CMOS Circuit Design”, John Wiley & Sons Ltd, 2004

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	2	-	1	1	-	-
CO2	2	-	1	1	-	-
CO3	2	-	2	1	-	-
CO4	2	-	1	1	-	-
CO5	2	-	2	1	2	-
CO	2	-	1	1	2	-

VL22103	**ADVANCED DIGITAL SYSTEM DESIGN**	**L**	**T**	**P**	**C**
		3	**0**	**2**	**4**

COURSE OBJECTIVES:

- To design synchronous sequential circuits.
- To understand about hazards and design in asynchronous sequential circuits.
- To learn how to test digital circuits for faults.
- To study the structure and working of programmable devices.
- To design and build digital circuits using software tools.

UNIT I	**SEQUENTIAL CIRCUIT DESIGN**	**9**

Analysis of Clocked Synchronous Sequential Circuits: A sequential Parity Checker, State Tables and Graphs, Reduction of State Tables and State Assignment, Design of Synchronous Sequential Circuits: Design Procedure, Design-Code Converter, Design of Iterative Circuits- Comparator.

UNIT II	**ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN**	**9**

Analysis of Asynchronous Sequential Circuit, Flow Table Reduction-Races-State Assignment-Transition Table and Problems in Transition Table- Design of Asynchronous Sequential Circuit - Static, Dynamic and Essential hazards, Designing Vending Machine Controller.

UNIT III	**FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS**	**9**

Fault Table Method, Path Sensitization Method, Boolean Difference Method, Fault Tolerance Techniques, Fault in PLA, Test Generation, DFT Schemes, Built in Self-Test.

UNIT IV	**SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES**	**9**

Programming Logic Device Families, Designing Synchronous Sequential Circuit using PLA/PAL, Designing ROM with PLA, Realization of Finite State Machine using PLD.

UNIT V	**SYSTEM DESIGN USING VERILOG**	**9**

Hardware Modeling with Verilog HDL – Logic System, Data Types and Operators for Modelling in Verilog HDL - Behavioral Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– Structural Modeling – Compilation and Simulation of Verilog Code – Test Bench - Realization of Combinational and Sequential Circuits using Verilog, Introduction to System Verilog.

45 PERIODS

PRACTICAL EXERCISES: 30 PERIODS

Experiments based on Verilog HDL/System Verilog

1.	Design of Registers.
2.	Design of Counters.
3.	Design of Sequential Machines.
4.	Design of Serial Adders, Multiplier and Divider.

TOTAL:75 PERIODS

COURSE OUTCOMES:	
Upon completion of the course, the students will be able to	
CO1:	Analyze and design synchronous sequential circuits.
CO2:	Analyze and design asynchronous sequential circuits.
CO3:	Illustrate the various fault diagnosis and testability techniques in digital circuits.
CO4:	Infer the design of synchronous circuits using programmable devices.
CO5:	Apply Verilog HDL for modeling, simulation, and synthesis of digital systems.
REFERENCES:	
1.	Charles H.Roth., "Fundamentals of Logic Design" Seventh Edition, Cengage Learning, 2014.
2.	M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999
3.	Nripendra N Biswas "Logic Design Theory" Prentice Hall of India, 2001.
4.	Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson, 2003.
5.	Paragk.Lala "Digital System Design Using PLD" B S Publications, 2003.
6.	S.Salivahanan, S. Arivazhagan," Digital circuits and Design, Oxford University Press, Fifth Edition, 2022.
7.	Stephen D Brown, "Fundamentals of digital logic", TMH publication, 2007.
8.	John M Yarbrough," Digital logic application and design" Thomas Learning, 2001.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	1	-	1	1	1	-
CO2	1	-	1	1	1	-
CO3	1	-	1	1	1	-
CO4	1	-	1	1	2	-
CO5	1	-	1	1	1	-
CO	1	-	1	1	1	-

VL22104	ANALOG IC DESIGN LABORATORY	L	T	P	C
		0	0	4	2
COURSE OBJECTIVES:					
• To learn industry standard Analog IC design					
• To learn practical design of Analog amplifiers, current mirror etc.					
• To learn the art of analog layout in IC design					
LIST OF EXPERIMENTS					
1.	Simulation of MOSFET IV characteristics and Extraction of second order parameters.				
2.	Design and Analysis of CMOS inverter.				
3.	Design and Analysis of basic single stage amplifiers (common source, common gate and common drain).				
4.	Design and Analysis of differential amplifier with active load and current source load.				
5.	Design and Analysis of simple current mirror and cascode current mirror.				
6.	Design and Analysis of two stage op-amp with frequency compensation.				
7.	Realize layout of CMOS inverter and perform post layout simulation.				
8.	Realize layout of CS amplifier with active load, with NMOS transistor as drive and PMOS transistor as load and perform post layout simulation.				
Lab Requirements: Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software.					
TOTAL: 60 PERIODS					
COURSE OUTCOMES:					
Upon completion of the course, the students will be able to					

CO1	Use EDA tools for Circuit Design
CO2	Design analog Circuit using CMOS given a design specification.
CO3	Design and carry out time domain and frequency domain simulations of simple analog building blocks.
CO4	Perform Pre-Layout Simulation and Post-Layout Simulation in analog circuits

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	2	-	2	2	2	-
CO2	2	-	2	2	2	-
CO3	2	-	2	3	2	-
CO4	2	-	2	3	2	-
CO5	2	-	2	2	2	-
CO	2	-	2	3	2	-

VL22105	**TECHNICAL SEMINAR**	**L**	**T**	**P**	**C**
		0	**0**	**2**	**1**

COURSE OBJECTIVES: In this course, students will develop their scientific and technical reading and writing skills that they need to understand and construct research articles. A term paper requires a student to obtain information from a variety of sources (i.e., Journals, dictionaries, reference books) and then place it in logically developed ideas. The work involves the following steps:

- Selecting a subject, narrowing the subject into a topic
- Stating an objective
- Collecting the relevant bibliography (atleast 15 journal papers)
- Preparing a working outline
- Studying the papers and understanding the authors contributions and critically analysing each paper
- Preparing a working outline
- Linking the papers and preparing a draft of the paper
- Preparing conclusions based on the reading of all the papers
- Writing the Final Paper and giving final Presentation

Please keep a file where the work carried out by you is maintained. Activities to be carried out

TOTAL: 30 PERIODS

METHOD OF EVALUATION:

Activity	Instructions	Submission week	Evaluation
Selection of area of interest and Topic Stating an Objective	You are requested to select an area of interest, topic and state an objective	2nd week	3 % Based on clarity of thought, current relevance and clarity in writing
Collecting Information about your area & topic	1. List 1 Special Interest Groups or professional society 2. List 2 journals 3. List 2 conferences, symposia or workshops 4. List 1 thesis title 5. List 3 web presences (mailing lists, forums, news sites) 6. List 3 authors who publish regularlyin your area 7. Attach a call for papers (CFP) from your area.	3rd week	3% (the selected information must be area specific and of international and national standard)
Collection of Journal	• You have to provide a	4th week	6% (the list of standard papers

papers in the topic in the context of the objective – collect20 & then filter	complete list of references you will be using- Based on your objective -Search various digital libraries and Google Scholar • When picking papers to read - try to: • Pick papers that are related to each other in some ways and/or that are in the same field so that you can write a meaningful survey out of them, • Favour papers from well-known journals and conferences, • Favour "first" or "foundational" papers in the field (as indicated in other people's survey paper), • Favour more recent papers, • Pick a recent survey of the field so you can quickly gain an overview, • Find relationships with respect to each other and to your topic area (classification scheme/categorization) • Mark in the hard copy of papers whether complete work or section/sections of the paper are being considered		and reason for selection)
Reading and notes for first 5 papers	Reading Paper Process • For each paper form a Table answering the following questions: What is the main topic of the article? • What was/were the main issue(s) the author said they want to discuss? • Why did the author claim it was important? • How does the work build on other's work, in the author's opinion? 5 th week 8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper) • What simplifying assumptions does the author claim to be making?	5th week	8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)

	• What did the author do? • How did the author claim they were going to evaluate their work and compare it to others? • What did the author say were the limitations of their research? • What did the author say were the important directions for future research? Conclude with limitations/issues not addressed by the paper (from the perspective of your survey)		
Reading and notes for next5 papers	Repeat Reading Paper Process	6th week	8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Reading and notes for final 5 papers	Repeat Reading Paper Process	7th week	8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Draft outline 1 and Linking papers	Prepare a draft Outline, your survey goals, along with a classification / categorization diagram	8th week	8% (this component willbe evaluated based on the linking and classification amongthe papers)
Abstract	Prepare a draft abstract and give a presentation	9th week	6% (Clarity, purpose andconclusion) 6% Presentation & Viva Voce
Introduction Background	Write an introduction and background sections	10th week	5% (clarity)
Sections of the paper	Write the sections of your paper based on the classification / categorization diagram in keeping with the goals of your survey	11th week	10% (this component willbe evaluated based on the linking and classification among the papers)
Your conclusions	Write your conclusions and future work	12th week	5% (conclusions – clarity and your ideas)
Final Draft	Complete the final draft of your paper	13th week	10% (formatting, English, Clarity andlinking) 4% Plagiarism Check Report
Seminar	A brief 15 slides on your paper	14th week & 15th week	10% (based on presentation and Viva-voce)

COURSE OUTCOMES:	
Upon completion of the course, the students will be able to	
CO1	Identify latest developments in the field of VLSI Design
CO2	Develop technical writing abilities for seminars, conferences and journal publications
CO3	Make use of modern tools to present the technical details

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	**Programme Outcomes**					
	1	**2**	**3**	**4**	**5**	**6**
CO1	3	-	3	-	-	3

CO2	-	3	1	-	-	3
CO3	-	-	1	-	-	3
CO	3	3	2	-	-	3

RM22101	**RESEARCH METHODOLOGY**	**L**	**T**	**P**	**C**
		2	**0**	**0**	**2**

COURSE OBJECTIVES:

- To give an overview of the research methodology and IPR, and explain the techniques of data collection and analysis

UNIT I	**RESEARCH DESIGN**	**6**

Overview of research process and design, Use of Secondary and exploratory data to answer the research question, Qualitative research, Observation studies, Experiments and Surveys.

UNIT II	**DATA COLLECTION AND SOURCES**	**6**

Measurements, Measurement Scales, Questionnaires and Instruments, Sampling and methods. Data - Preparing, Exploring, examining and displaying.

UNIT III	**DATA ANALYSIS AND REPORTING**	**6**

Overview of Multivariate analysis, Hypotheses testing and Measures of Association. Presenting Insights and findings using written reports and oral presentation.

UNIT IV	**INTELLECTUAL PROPERTY RIGHTS**	**6**

Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.

UNIT V	**PATENTS**	**6**

Patents – objectives and benefits of patent, Concept, features of patent, Inventive step, Specification, Types of patent application, process E-filling, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licences, Licensing of related patents, patent agents, Registration of patent agents.

TOTAL: 30 PERIODS

COURSE OUTCOMES:

Upon completion of the course, the students will be able to

CO1:	Outline the methodology of research
CO2:	Explain the research design, data collection methods, IPR and patent
CO3:	Prepare a well-structured research paper, scientific presentations and patent applications
CO4:	Develop awareness on IPR, patent law and procedural mechanism in obtaining a patent
CO5:	Compare the methods of measurement scale, questionnaire, sampling and data analysis

REFERENCES:

1.	Cooper Donald R, Schindler Pamela S and Sharma JK, “Business Research Methods”, Tata McGraw Hill Education, 11e (2012).
2.	Kothari C R, Gaurav Garg, “Research Methodology- Methods and Techniques” New Age International Publishers, 2019.
3.	Catherine J. Holland, “Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets”, Entrepreneur Press, 2007.
4.	David Hunt, Long Nguyen, Matthew Rodgers, “Patent searching: tool & techniques”, Wiley, 2007
5.	The Institute of Company Secretaries of India, Statutory body under an Act of parliament, “Professional Programme Intellectual Property Rights, Law and practice”, 2013.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	**Programme Outcomes**					
	1	**2**	**3**	**4**	**5**	**6**
CO1	-	-	3	-	-	-
CO2	-	-	3	-	-	-
CO3	-	2	3	-	-	-
CO4	-	-	3	-	-	-
CO5	-	-	3	-	-	2
CO	-	2	3	-	-	2

SEMESTER II

VL22201	DIGITAL CMOS VLSI DESIGN	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To learn the CMOS basics in digital circuits.
- To design CMOS-based combinational circuits.
- To design CMOS-based sequential circuits.
- To apply various CMOS logic styles and techniques to optimize digital subsystems.
- To evaluate and estimate circuit performance.

UNIT I	MOS TRANSISTORS AND CMOS INVERTER	9

MOS transistor characteristics, short channel effects, CMOS inverter design, stick diagrams, power, delay, sizing.

UNIT II	COMBINATIONAL LOGIC CIRCUITS	9

Complementary CMOS, power reduction, ratioed logic, pass transistor logic, dynamic CMOS, Domino, NP-CMOS.

UNIT III	SEQUENTIAL CIRCUITS	9

Static latches and registers, dynamic latches and registers, flip-flops, clocking strategies, Schmitt trigger, monostable, astable circuits.

UNIT IV	CMOS SUB SYSTEM DESIGN	9

Adders (carry bypass, select, CLA), multipliers, counters, parity generators, multiplexers, shifters, memory elements.

UNIT V	PERFORMANCE ESTIMATION & DESIGN TECHNIQUES	9

Delay estimation, logical effort, sizing, power, interconnects, scaling, synchronous and self-timed design.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of the course, the students will be able to

CO1	Explain CMOS basics in digital circuits.
CO2	Design CMOS-based combinational circuits.
CO3	Design CMOS-based sequential circuits.
CO4	Apply various CMOS logic styles and techniques to optimize digital subsystems.
CO5	Evaluate and estimate circuit performance.

REFERENCES:

1.	Weste, N. H. E., & Harris, D. "CMOS VLSI design: A circuits and systems perspective. Pearson", 2011.
2.	Rabaey, J. M., & Nikolić, B. "Digital integrated circuits". Pearson, 2003.
3.	Martin, K. "Digital integrated circuit design". Oxford University Press, 2011.
4.	Palnitkar, S. "Verilog HDL" (2nd ed.). Pearson Education, 2003.
5.	Rabaey, J. M., Chandrakasan, A., & Nikolić, B, "Digital integrated circuits", Pearson, 2003.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	2	-	2	1	2	1
CO2	2	-	2	1	2	1
CO3	2	-	2	1	2	1
CO4	2	-	2	1	2	1
CO5	2	-	2	1	2	1
CO	2	-	2	1	2	1

VL22202	DESIGN FOR VERIFICATION USING UVM	L	T	P	C
		3	0	2	4

COURSE OBJECTIVES:

- To provide the students complete understanding on UVM testing
- To become proficient at UVM verification
- To provide an experience on self-checking UVM testbenches

UNIT I	UVM & TRANSACTION-LEVEL MODELING	9

Overview- The Typical UVM Testbench Architecture- The UVM Class Library-Transaction-Level Modeling (TLM) -Overview- TLM, TLM-1, and TLM-2.0 -TLM-1 Implementation- TLM-2.0 Implementation

UNIT II	DEVELOPING REUSABLE VERIFICATION COMPONENTS	9

Modeling Data Items for Generation - Transaction-Level Components - Creating the Driver - Creating the Sequencer - Connecting the Driver and Sequencer -Creating the Monitor - Instantiating Components- Creating the Agent - Creating the Environment –Enabling Scenario Creation -Managing of Test- Implementing Checks and Coverage

UNIT III	UVM USING VERIFICATION COMPONENTS	9

Creating a Top-Level Environment- Instantiating Verification Components - Creating Test Classes - Verification Component Configuration - Creating and Selecting a User-Defined Test – Creating Meaningful Tests- Virtual Sequences- Checking for DUT Correctness- Scoreboards- Implementing a Coverage Model

UNIT IV	UVM USING THE REGISTER LAYER CLASSES	9

Constructing a Register Model - Back-Door Access -Special Registers -Integrating a Register- Model in a Verification Environment- Integrating a Register Model- Randomizing Field Values- Pre-Defined Sequences

UNIT V	UBUS VERIFICATION COMPONENT EXAMPLE	9

UBus Example, UBus Example Architecture, UBus Top Module, The Test, Testbench Environment, UBus Environment, UBus Master Sequencer, UBus Driver, UBus Agent Monitor, Ubus Interface

45 PERIODS

PRACTICAL EXCERCISES: 30 PERIODS

1.	Simulate a simple UVM testbench and DUT
2.	Design and simulate sequence items and sequence
3.	Design and simulate a UVM driver and sequencer
4.	Design and simulating UVM monitor and agent
5.	Design, simulate and examine coverage
6.	Design and simulate a UVM scoreboard and environment, and verifying the outputs of a (faulty) DUT

TOTAL:75 PERIODS

COURSE OUTCOMES:

Upon completion of the course, the students will be able to

CO1	Apply UVM concept and transaction-level modeling to build a basic UVM testbench.
CO2	Develop reusable verification components.
CO3	Apply UVM components to create configurable test environments.
CO4	Construct UVM reister models using back-door access to verify register operations.
CO5	Implement and verify a complete UBus based verification environment.

REFERENCES:

1.	"Universal Verification Methodology (UVM)1.2 User's Guide", Accellera System Initiative, 2015.
2.	Srivatsa Vasudevan, "Practical UVM: Step by Step Examples" with IEEE 1800.2, R.R. Bowker, Second Edition, 2020.
3.	Chris Spear, Greg Tumbush, "SystemVerilog for Verification: A Guide to Learning the Testbench Language Features", Third Edition, 2014.
4.	Ray Salemi, "The UVM Primer, An Introduction to the Universal Verification Methodology", 2013.
5.	Vanessa R Cooper, "Getting started with UVM: A Beginner's Guide", 2013.

Mapping of Course Outcomes with Program Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	3	1	2	2	2	2
CO2	3	1	2	2	2	2
CO3	3	1	2	2	2	2
CO4	3	1	2	2	2	2
CO5	3	1	2	2	2	2
CO	3	1	2	2	2	2

VL22203	**ASIC DESIGN**	**L**	**T**	**P**	**C**
		3	**0**	**2**	**4**

COURSE OBJECTIVES:

- To prepare the student to be an entry-level industrial standard ASIC or FPGA designer.
- To analyze the issues and tools related to ASIC/FPGA design and implementation.
- To understand basics of System on Chip and Platform based design.

UNIT I	**INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN**	**9**

Types of ASICs - Design Flow - CMOS Transistors - Combinational Logic Cell - Sequential Logic Cell - Data Path Logic Cell - Transistors as Resistors - Transistor Paracitic Capacitance - Logical Effort.

UNIT II	**PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS**	**9**

Anti Fuse - Static RAM - EPROM and EEPROM Technology - ACTEL ACT - Xilinx LCA - ALTERA FLEX - ALTERA MAX DC & AC Inputs and Outputs - Clock and Power Inputs - Xilinx I/O Blocks.

UNIT III	**PROGRAMMABLE ASIC ARCHITECTURE**	**9**

Architecture and Configuration of ARTIX / Cyclone and KINTEX Ultra Scale / STRATIX FPGA – Micro-Blaze / NIOS Based Embedded Systems – Signal Probing Techniques.

UNIT IV	**LOGIC SYNTHESIS, PLACEMENT AND ROUTING**	**9**

Logic Synthesis - Floor Planning Goals and Objectives, Measurement of Delay in Floor Planning, Floor Planning Tools, I/O and Power Planning, Clock Planning, Placement Algorithms. Routing: Global Routing, Detailed Routing, Special Routing.

UNIT V	**SYSTEM-ON-CHIP DESIGN**	**9**

SoC Design Flow, Platform-Based and IP Based SoC Designs, Basic Concepts of Bus-Based Communication Architectures, High Performance Filters using Delta-Sigma Modulators. Case Studies: Digital Camera, SDRAM, High Speed Data standards.

45 PERIODS

PRACTICAL EXCERCISES: 30 PERIODS

1.	Simulate CMOS inverter circuits and study transistor parasitic effects using a circuit simulator.
2.	Design a 4 bit RCA using data flow modeling.
3.	Design a 16 bit accumulator using behavioral modeling.
4.	Design of an 8 bit datapath using a 4:1 MUX, Register and shift register with structural modeling.
5.	FPGA implementation of a simple ALU model.

TOTAL:75 PERIODS

COURSE OUTCOMES:

Upon completion of the course, the students will be able to

CO1	Apply logical effort technique for predicting delay, delay minimization and FPGA architectures
CO2	Design logic cells and I/O cells.
CO3	Analyze the various resources of recent FPGAs.
CO4	Use algorithms for Floor planning and Placement of Cells and to apply the routing algorithms
CO5	Analyze high performance Algorithms available for ASICs.

REFERENCES:

1.	M.J.S.Smith, "Application Specific Integrated Circuits", Pearson, 2003.
2.	Steve Kilts, “Advanced FPGA Design,” Wiley Inter-Science,2006 .
3.	Douglas J. Smith, HDL Chip Design, Madison, AL, USA: Doone Publications, 1996.
4.	Chan, K., & Mourad, S., "Digital Design using Field Programmable Gate Array", Prentice Hall, 1994.
5.	Nekoogar, F. (1999), Timing verification of application specific integrated circuit (ASICs), Prentice Hall,1999.
6.	H.Gerez, “Algorithms for VLSI Design Automation”, John Wiley,1999.
7.	Wolf, W.,”FPGA base system design”, Prentice Hall, 2004.

Mapping of Course Outcomes with Program Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	3	2	2	3	2	2
CO2	3	2	2	2	3	2
CO3	3	3	2	2	3	3
CO4	3	2	2	3	2	3
CO5	3	3	2	2	2	3
CO	3	2	2	2	2	3

VL22204	**LOW POWER VLSI DESIGN**	**L**	**T**	**P**	**C**
		3	**0**	**2**	**4**

COURSE OBJECTIVES:

- To identify the sources of power used in an IC.
- To identify the power reduction techniques based on technology independent and technology dependent.
- To describe how power is lost in different MOS logic circuits.
- To choose appropriate techniques to minimize power loss in digital circuits.
- To design memory circuits that use less power.

UNIT I	**POWER DISSIPATION IN CMOS**	**9**

Sources of power Dissipation, Physics of Power Dissipation in CMOS FET Devices – Physics of Power Dissipation in MOSFET Devices- Power Dissipation in CMOS – Hierarchy of limits of power – Basic Principle of Low Power Design.

UNIT II	**POWER OPTIMIZATION**	**9**

Gate Level Low Power Design –Architecture Level Low Power Design – VLSI Subsystem Design of Adders, Multipliers, Low Voltage Circuit Design Techniques.

UNIT III	**DESIGN OF LOW POWER CMOS CIRCUITS**	**9**

Computer Arithmetic Techniques for Low Power System – Reducing Power Consumption in Combinational Logic, Sequential Logic, Memories – Low Power Clock – Advanced Techniques – Special Techniques, Adiabatic Techniques.

UNIT IV	**POWER ESTIMATION**	**9**

Power Estimation Techniques, Circuit Level, Gate Level, Architecture Level, Behavioral Level, – Logic Power Estimation – Simulation Power Analysis –Probabilistic Power Analysis.

UNIT V	**SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER**	**9**

Synthesis for Low Power – Behavioral Level Transform – Logic level Optimization for Low Power – Software Design for Low Power.

45 PERIODS

PRACTICAL EXCERCISES: 30 PERIODS

1.	Power Estimation at Circuit, Transistor and Gate Levels in CMOS Logic.
2.	Low Power Optimization Techniques for Combinational CMOS Logic Circuits.
3.	Low Power Optimization Techniques for Sequential CMOS Logic Circuits.
4.	Power Optimization at Register-Transfer Level Using Behavioral Transformations.

5.	Power Optimization at Algorithmic Level Using Low-Power Computational Techniques.
	TOTAL:75 PERIODS
COURSE OUTCOMES:	
Upon completion of the course, the students will be able to	
CO1	Explain the physical reasons behind power dissipation in CMOS FET devices.
CO2	Identify suitable multiplier architectures for low-power applications.
CO3	Apply low-power techniques to clock and interconnect design.
CO4	Apply power estimation techniques at various design levels using simulation and probabilistic methods.
CO5	Develop simple low-power system modules using synthesis and software methods.
REFERENCES:	
1.	Kaushik Roy and S.C.Prasad, "Low Power CMOS VLSI Circuit Design", Wiley, 2009
2.	Ajit Pal, "Low-Power VLSI Circuits and Systems", Springer, August, 2016.
3.	Anantha Chandrakasan, "Low Power CMOS Design", IEEE Press, /Wiley International, 1998.
4.	J.Rabaey, "Low Power Design Essentials (Integrated Circuits and Systems)", Springer, 2009.
5.	J.B.Kulo and J.H Lou, "Low Voltage CMOS VLSI Circuits", Wiley 2017.
6.	James B.Kulo, Shih-Chia Lin, "Low Voltage SOI CMOS VLSI Devices and Circuits", John Wiley and Sons, Inc. 2001.
7.	J.Rabaey, "Low Power Design Essentials (Integrated Circuits and Systems)", Springer, 2009.

Mapping of Course Outcomes with Program Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	2	1	2	3	2	1
CO2	2	1	2	2	2	1
CO3	1	1	2	2	2	1
CO4	1	1	2	3	2	1
CO5	2	1	2	2	3	1
CO	2	1	2	2	2	1

VL22205	**FPGA LABORATORY**	**L**	**T**	**P**	**C**
		0	**0**	**4**	**2**

COURSE OBJECTIVES:	
• To equip learners with a comprehensive understanding of System Verilog language constructs for digital design and verification	
• To develop proficiency in creating testbenches and applying advanced verification techniques	
• To familiarize students with FPGA development tools, thereby bridging the gap between simulation and real-world FPGA deployment.	
LIST OF EXPERIMENTS:	
1.	Introduction to System Verilog: Design, Simulation, and Verification Techniques.
2.	Model and verify a 4-bit Binary Adder.
3.	Model and test a 4-bit Arithmetic Logic Unit (ALU).
4.	Implementation of Multiplexer and Demultiplexer with Blocking and Non-blocking Assignments.
5.	Implementation of Finite State Machine-Based Sequence Detector with 2-State and 4-State Enumerated Types.
6.	Design and Verification of Digital Counters (Up, Down, Ring).
7.	Study of System Verilog Testbench for Simulation and Validation of Hardware Designs.
8.	Develop a test program to verify the functional correctness of encoder and decoder

	designed.
9.	Testbench verification of read and write operation in memory.
10.	Study of functional verification using Dynamic Array Scoreboard.
11.	Study of Mailboxes for Synchronization and Data Transfer in Verification.
12.	Study of Scalable System Verilog Testbenches with Basic and Advanced OO Methodologies.
LAB REQUIREMENTS: Vivado Design Suite or equivalent Xilinx FPGA EDA tools along with Xilinx or equivalent FPGA development boards	
	TOTAL: 60 PERIODS
COURSE OUTCOMES:	
Upon completion of the course, the students will be able to	
CO1	Demonstrate the fundamental understanding of System Verilog design constructs.
CO2	Implement basic combinational and sequential digital circuits using System Verilog.
CO3	Develop Verilog test environments of significant capability and complexity.
CO4	Utilize advanced System Verilog verification features including dynamic arrays, mailboxes, scoreboards, and object-oriented methodologies to create robust test environments.

Mapping of Course Outcomes with Program Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	2	1	2	2	2	2
CO2	2	1	2	2	2	2
CO3	2	1	2	2	2	2
CO4	2	1	2	2	2	2
CO5	2	1	2	2	2	2
CO	2	1	2	2	2	2

RM22201	**RESEARCH TOOL LABORATORY**	**L**	**T**	**P**	**C**
		0	**0**	**4**	**2**
COURSE OBJECTIVES:					
• To familiarize the fundamental concepts/techniques for Project Management					
• To familiarize the journal paper formatting using suitable Software					
• To familiarize the software for literature review and Bibliography					
• To find the plagiarism percentage of article contents					
• To prepare a quality research report and the presentation					
LIST OF EXPERIMENTS:					
1.	Use of tools / Techniques for Research - Project management -Microsoft Project / Microsoft OneNote / Asana.				
2.	Hands on training related to software for paper formatting like LaTeX / MS Office				
3.	Design a layout of a research paper - Guidelines for submitting the research paper - Review process -Addressing reviewer comments.				
4.	Design and simulate a UVM driver and sequencer				
5.	Introduction to Data Analysis Software - Origin SPSS, ANOVA etc.,				
6.	Introduction to software for detection of plagiarism – Urkund, Turniton				
7.	Preparing bibliography / Different reference formats. – EndNote, Mently				
8.	Format of project report - Use of quotations - Method of transcription- Elements: Title Page - Abstract - Table of Contents - Headings and Sub-Headings – Footnotes - Tables and Figures				
9.	Introduction to Microsoft Excel –for research analysis				
10.	Presentation using PPTs.				
	TOTAL: 60 PERIODS				

COURSE OUTCOMES:	
Upon completion of the course, the students will be able to	
CO1	List the various stages in research and develop systematic planning of project stages.
CO2	Write a journal paper and formulate as per the standard journal format (Applying)
CO3	Develop a literature review and relevant references for a research problem using suitable software.
CO4	Determine the plagiarism of the article/report content by using the Software (Applying)
CO5	Compile a research report and the presentation (Applying)

Mapping of Course Outcomes with Program Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	2	2	-	-	-	-
CO2	-	2	-	-	-	-
CO3	1	2	1	-	-	-
CO4	-	2	1	-	-	-
CO5	-	2	1	-	-	-
CO	2	2	1	-	-	-

SEMESTER III

VL222301	INPLANT / INDUSTRIAL / PRACTICAL TRAINING	L	T	P	C
		0	0	4	2
COURSE OBJECTIVES:					
• To train the students in the field work so as to have first – hand knowledge of practical problems related to VLSI design in carrying out engineering tasks.					
SYLLABUS:					
The students individually undertake training in reputed companies /organization during the summer vacation for a specified duration of four weeks. At the end of training, a detailed report on the work done should be submitted within ten days from the commencement of the semester. The students will be evaluated through a viva-voce examination by a team of internal staff.					
TOTAL: 120 PERIODS					

VL222302	PROJECT WORK I	L	T	P	C
		0	0	6	3
COURSE OBJECTIVES:					
• To identify a specific problem for the current need of the society and collecting information related to the same through detailed review of literature.					
• To develop the methodology to solve the identified problem.					
• To train the students in preparing project reports and to face reviews and viva-voce examination.					
SYLLABUS:					
The student individually works on a specific topic approved by faculty member who is familiar in this area of interest. The student can select any topic which is relevant to his/her specialization of the programme. The topic may be experimental or analytical or case studies. At the end of the semester, a detailed report on the work done should be submitted which contains clear definition of the identified problem, detailed literature review related to the area of work and methodology for carrying out the work. The students will be evaluated through a viva-voce examination by a panel of examiners including one external examiner.					
TOTAL: 120 PERIODS					
COURSE OUTCOMES:					
Upon completion of the course, the students will be able to					

CO1	Discover potential research areas.
CO2	Apply the knowledge gained from theoretical and practical courses to be creative, well-planned, organized and coordinated.
CO3	Represent data acquired in graphical and reader-friendly formats.
CO4	Derive detailed conclusions from work carried out.

Mapping of Course Outcomes with Program Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	3	3	3	3	3	3
CO2	3	3	3	3	3	3
CO3	3	3	3	3	3	3
CO4	3	3	3	3	3	3
CO	3	3	3	3	3	3

SEMESTER IV

VL222401	**PROJECT WORK II**	**L**	**T**	**P**	**C**
		0	**0**	**24**	**12**

COURSE OBJECTIVES:

- To solve the identified problem based on the formulated methodology.
- To develop skills to analyze and discuss the test results, and make conclusions

SYLLABUS:

The student should continue the phase I work on the selected topic as per the formulated methodology / Undergo internship. At the end of the semester, after completing the work to the satisfaction of the supervisor and review committee, a detailed report should be prepared and submitted to the head of the department. The students will be evaluated based on the report and the viva-voce examination by a panel of examiners including one external examiner.

TOTAL: 360 PERIODS

COURSE OUTCOMES:

Upon completion of the course, the students will be able to

CO1	Discover potential research areas.
CO2	Apply the knowledge gained from theoretical and practical courses to be creative, well-planned, organized and coordinated.
CO3	Represent data acquired in graphical and reader-friendly formats.
CO4	Derive detailed conclusions from work carried out.
CO5	Report and present the findings of the work conducted

Mapping of Course Outcomes with Program Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	3	3	3	3	3	3
CO2	3	3	3	3	3	3
CO3	3	3	3	3	3	3
CO4	3	3	3	3	3	3
CO5	3	3	3	3	3	3
CO	3	3	3	3	3	3

PROFESSIONAL ELECTIVES

SEMESTER II, PROFESSIONAL ELECTIVE – I

VL22211	CMOS FABRICATION TECHNOLOGY	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To understand IC processing basics and bipolar/NMOS/CMOS technologies.
- To acquire knowledge on crystal structure, process of crystal growth, properties of materials used for crystal and examine the technique suitable for specific applications.
- To understand epitaxy and film deposition methods.
- To apply oxidation and diffusion models to doping.
- To apply Lithography, Etching, and Metallization solutions.

UNIT I	VLSI PROCESS INTEGRATION	9

Fundamental Considerations for IC Processing, Bipolar IC Technology NMOS IC Technology, CMOS IC Technology, Modern IC Fabrication.

UNIT II	CRYSTAL GROWTH AND WAFER PREPARATION	9

Electronic grade Silicon, Czochralski Crystal Growing, Silicon Shaping, Processing Considerations.

UNIT III	EPITAXY AND POLYSILICON FILM DEPOSITION	9

Vapor -Phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Deposition Process, Plasma assisted Deposition.

UNIT IV	OXIDATION AND DIFFUSION	9

Growth Mechanism and Kinematics, Oxidation Techniques and Systems, Oxidation of Polysilicon, Models of Diffusion in Solid, Fick's One-Dimensional Diffusion Equations, Atomistic Diffusion Mechanisms.

UNIT V	LITHOGRAPHY, ETCHING AND METALLIZATION	9

Lithographic process, Optical Lithography, Electron beam Lithography, Dry etching process for VLSI technology, Metallization Problems, Metallization Failure.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of the course, the students will be able to

CO1	Illustrate the different process integration technologies for IC fabrication.
CO2	Explain crystal growth and wafer shaping.
CO3	Explain epitaxy types and polysilicon processes.
CO4	Apply oxidation techniques and diffusion for dopant profiles.
CO5	Apply lithography, dry etching, and metallization to resolve VLSI issues.

REFERENCES:

1.	S.M.Sze, "VLSI Technology", Second Edition, Mc.Graw Hill, 2017.
2.	S.A.Campbell, “The Science of Micro Electronic Fabrication”, Oxford series, Second Edition, 2012.
3.	Douglas A. Pucknell and Kamran Eshraghian, " Basic VLSI Design", Prentice Hall India, 2003.
4.	Wayne Wolf, Modern VLSI Design: IP-Based Design, 4th Edition, Pearson Education, 2016.
5.	Amar Mukherjee, "Introduction to NMOS and CMOS VLSI System design’, Prentice Hall India, 2000.
6.	Plummer, Deal and Griffin, “Silicon VLSI Technology Fundamentals, Practice and Modeling”, Prentice Hall Series, 2012.
8.	C.Y. Chang and S.M.Sze (Eds) , “ULSI Technology”, McGraw Hill Companies Inc., 1996.

Mapping of Course Outcomes with Program Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	2	2	2	1	1	2
CO2	2	2	2	1	1	2
CO3	2	2	2	1	1	2

CO4	2	2	2	1	1	2
CO5	2	2	2	1	1	2
CO	2	2	2	1	1	2

VL22112	**ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To gain broad conceptual understanding of the various aspects of electromagnetic (EM) interference and compatibility
- To develop a theoretical understanding of electromagnetic shielding effectiveness
- To understand ways of mitigating EMI by using shielding, grounding and filtering
- To understand the need for standards and to appreciate measurement methods
- To understand how EMI impacts wireless and broadband technologies

UNIT I	**SOURCES OF EM INTERFERENCE**	**9**

Classification of sources - Natural sources - Man-made sources - Survey of theelectromagnetic environment.

UNIT II	**EM SHIELDING**	**9**

Shielding Theory- LF Magnetic shielding, PCB level Shielding- Shielding effectiveness - Far-field sources - Near-field sources - Low-frequency,magnetic field shielding - Effects of apertures.

UNIT III	**INTERFERENCE CONTROL TECHNIQUES**	**9**

Equipment screening - Cable screening - grounding - Power-line filters - Isolation - Balancing -Signal-line filters - Nonlinear protective devices.

UNIT IV	**EMC STANDARDS, MEASUREMENTS AND TESTING**	**9**

Need for standards - Civilian EMC standards – Military standards - The international framework - Human exposure limits to EM fields -EMC measurement techniques - Measurement tools - Test environments.

UNIT V	**EMC CONSIDERATIONS IN WIRELESS AND BROAD BAND TECHNOLOGIES**	**9**

Efficient use of frequency spectrum - EMC, interoperability and coexistence - Specifications and alliances - Transmission of high-frequency signals over telephone and power networks — EMC and digital subscriber lines - EMC and power line telecommunications.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of the course, the students will be able to

CO1	Apply knowledge of the various sources of electromagnetic interference to identify and categorize interference in practical engineering scenarios.
CO2	Identify principles of electromagnetic coupling through apertures to solve basic problems involving field interactions and interference effects.
CO3	Analyze different EMI mitigation techniques, including shielding and grounding, to determine their effectiveness in reducing interference.
CO4	Examine the need for electromagnetic compatibility (EMC) standards and interpret key EMC measurement methods for compliance evaluation.
CO5	Inspect the impact of electromagnetic compatibility on wireless and broadband technologies, identifying challenges and potential performance issues.

REFERENCES:

1.	Christopoulos C, " Principles and Techniques of Electromagnetic Compatibility", CRC Press,Second Edition, Indian Edition, 2013.
2.	Paul C R, "Introduction to Electromagnetic Compatibility", Wiley India, Third Edition, 2022.
3.	Kodali V P, "Engineering Electromagnetic Compatibility", Wiley India, Second Edition, 2010.
4.	Henry W Ott, " Electromagnetic Compatibility Engineering", John Wiley & Sons Inc, Newyork, 2009.
5.	Scott Bennett W, "Control and Measurement of Unintentional Electromagnetic Radiation", John Wiley& Sons Inc., Wiley Interscience Series, 1997.
6.	David A. Weston, "Electromagnetic Compatibility: Principles and Applications", CRC Press, Second Edition, 2017.

Mapping of Course Outcomes with Program Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	3	-	2	2	1	-
CO2	2	-	2	3	1	-
CO3	2	1	2	2	3	-
CO4	2	3	-	2	1	2
CO5	2	-	-	3	1	2
CO	2	2	2	2	1	2

VL22213	**ADVANCED WIRELESS SENSOR NETWORKS**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To understand the fundamental concepts, challenges, and application areas of wireless sensor networks.
- To study the architecture, hardware, and energy aspects of sensor nodes and their network organization.
- To explore various MAC and routing protocols used in wireless sensor networks for efficient communication.
- To analyze infrastructure establishment techniques such as topology control, synchronization, and localization.
- To examine data management, aggregation, and security mechanisms for reliable and secure WSN operation.

UNIT I	**FUNDAMENTALS OF WIRELESS SENSOR NETWORKS**	**9**

Challenges for wireless sensor networks-characteristics requirements-required mechanisms, difference between mobile ad-hoc and sensor networks, applications of sensor networks- case study, enabling technologies for wireless sensor networks.

UNIT II	**SENSOR NODE AND NETWORK ARCHITECTURES**	**9**

Single-node architecture - hardware components, energy consumption of sensor nodes , operating systems and execution environments, network architecture - sensor network scenarios, optimization goals and figures of merit, gateway concepts. Physical layer and transceiver design considerations.

UNIT III	**MEDIUM ACCESS AND ROUTING PROTOCOLS FOR WSN**	**9**

MAC protocols for wireless sensor networks, IEEE 802.15.4, Zigbee, low duty cycle protocols and wakeup concepts - s-MAC , the mediation device protocol, wakeup radio concepts, address and name management, assignment of MAC addresses, routing protocols- energy- efficient routing, geographic routing.

UNIT IV	**INFRASTRUCTURE ESTABLISHMENT**	**9**

Topology control, clustering, time synchronization, localization and positioning, sensor tasking and control.

UNIT V	**DATA HANDLING, AGGREGATION, AND SECURITY IN WSN**	**9**

Data management in WSN, storage and indexing in sensor networks, query processing in sensor, data aggregation, directed diffusion, tiny aggregation, greedy aggregation, security in WSN, security protocols for sensor networks, secure charging and rewarding scheme, secure event and event boundary detection.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of the course, the students will be able to

CO1	Use WSN fundamentals and technologies for practical applications.
CO2	Implement sensor node and network architectures efficiently.
CO3	Configure MAC and routing protocols for energy-efficient communication.
CO4	Deploy topology control, clustering, and localization techniques.
CO5	Demonstrate data aggregation and security mechanisms in WSNs.

REFERENCES:

1.	Fei Hu & Xiaojun Cao, “Wireless Sensor Networks: Principles and Practice”,CRC Press / Taylor & Francis, 2010

2.	Yingshu Li, My T. Thai,Weili Wu, “Wireless Sensor Networks and Applications”, Springer, 2008.
3.	Erdal Çayirci , Chunming Rong, “Security in Wireless Ad Hoc and Sensor Networks”, John Wiley and Sons, 2009.
4.	Shuang-Hua Yang, “Wireless Sensor Networks: Principles, Design and Applications”, Springer, London 2014.
5.	Hossam Mahmoud A. Fahmy, “Wireless Sensor Networks: Concepts, Applications, Experimentation and Analysis”,Springer, Singapore, 2016

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	1	-	1	1	1	-
CO2	1	-	1	1	1	-
CO3	1	-	1	1	1	-
CO4	1	-	1	1	1	-
CO5	1	-	1	1	1	-
CO	1	-	1	1	1	-

VL22214	**HARDWARE SOFTWARE CO-DESIGN FOR FPGA**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To acquire the knowledge about system specification and modelling
- To learn the formulation of partitioning
- To study the different technical aspects about prototyping and emulation

UNIT I	**SYSTEM SPECIFICATION AND MODELLING**	**9**

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling, Co-Design for Heterogeneous Implementation - Processor Synthesis, Single-Processor Architectures with One ASIC, Single-Processor Architectures with Many ASICs, Multi-Processor Architectures.

UNIT II	**HARDWARE/SOFTWARE PARTITIONING**	**9**

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of The Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning Based On Heuristic Scheduling, HW/SW Partitioning Based on Genetic Algorithms.

UNIT III	**HARDWARE/SOFTWARE CO-SYNTHESIS**	**9**

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.

UNIT IV	**PROTOTYPING AND EMULATION**	**9**

Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping, Target Architecture, Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems.

UNIT V	**DESIGN SPECIFICATION AND VERIFICATION**	**9**

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design System-Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Multi-Language Co-Simulation.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of the course, the students will be able to

CO1	Describe hardware software system architectures and design methodologies.
CO2	Discuss the hardware/software partitioning problem including cost estimation, heuristic scheduling, and genetic algorithms.
CO3	Implement the principles of hardware-software co-synthesis to partition system functions and optimize performance for a specific embedded application.

CO4	Construct functional hardware-software prototypes using modern EDA (Electronic Design Automation) tools and FPGA-based development platforms.
CO5	Execute system-level modelling and co-simulation using specialized languages to validate the synchronization between hardware and software components.

REFERENCES:

1.	Patrick Schaumont, "A Practical Introduction to Hardware/SoftwareCo-design",Springer,2010.
2.	Frank Vahid and Tony D. Givargis, "Embedded System Design: A Unified Hardware/Software Introduction," 3rd Edition, Wiley, 2018.
3.	Rainer Leupers and Peter Marwedel, "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems", Springer, 2012
4.	Jorgen Staunstrup, Wayne Wolf, "Hardware/Software Co-Design: Principles and Practice",Kluwer Academic Publisher,1997.
5.	Giovanni De Micheli, Rolf Ernst Morgon, "Reading in Hardware/Software Co-Design", Kaufmann Publisher,2001
6.	Gabriela Nicolescu and Pieter J. Mosterman, "Model-Based Design for Embedded Systems", CRC Press, 2018.

Mapping of Course Outcomes with Program Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	2	2	2	2	-	1
CO2	2	2	2	2	-	1
CO3	2	2	2	2	2	2
CO4	2	2	2	1	2	2
CO5	2	2	2	1	2	2
CO	2	2	2	2	2	2

VL22215	**HARDWARE SECURITY**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To provide a solid understanding of fundamental concepts in Cryptography.
- To have knowledge of designing finite field arithmetic on FPGA.
- To design and implement efficient elliptic curve scalar multiplication on FPGAs.
- To understand side channel attacks.
- To have knowledge of Physically Unclonable Function.

UNIT I	**FUNDAMENTALS OF CRYPTOGRAPHY**	**9**

Mathematical background for cryptography and introduction to hardware security. Symmetric key ciphers: AES. Asymmetric Key Ciphers: RSA cryptosystem, Elliptic curve cryptography. Hardware design of AES

UNIT II	**DESIGN OF FINITE FIELD ARITHMETIC ON FPGAS**	**9**

Finite Field Multiplier, Karatsuba Multipliers for Elliptic Curves, Analyzing Karatsuba Multipliers on FPGA Platforms, Finite Field Inversion Architecture for FPGAs, Itoh-Tsujii Inversion Algorithm, the Quad ITA Algorithm. Generalization of the ITA for 2^n Circuit, Hardware Architecture for 2^n Circuit Based ITA, Area and Delay Estimations for the 2^n ITA, Obtaining the Optimal Performing ITA Architecture.

UNIT III	**IMPLEMENTATION OF ELLIPTIC CURVE SCALAR MULTIPLICATION ON FPGAS**	**9**

The Elliptic Curve Cryptoprocessor, Point Arithmetic on the ECCP, The Finite State Machine (FSM), Performance Evaluation, Acceleration Techniques of the ECC Processor, Pipelining Strategies for Scalar Multiplier, Scheduling of the Montgomery Algorithm, Finding the Right Pipeline, Detailed Architecture of the ECM, Implementation Results.

UNIT IV	**SIDE CHANNEL ATTACKS**	**9**

Types of Side Channel Attacks, Kocher's Seminal Works, Power Attacks, Fault Attacks, Cache Attacks, Scan Chain-Based Attacks. Case Study: Impact of Side-Channel Attacks on Secure Embedded Hardware in Engineering Applications.		
UNIT V	**PHYSICALLY UNCLONABLE FUNCTIONS**	**9**
Basics of Physically Unclonable Functions **(**PUFs), Attacks on PUFs and PUF-based Systems, PUF implementations and Evaluation, PUF-based Cryptographic Protocols, Security Model for PUF-based Systems. Case Study: Evaluating the Impact of Aging on Silicon- Based Physically Unclonable Functions (PUFs).		
		TOTAL: 45 PERIODS
COURSE OUTCOMES:		
Upon completion of the course, the students will be able to		
CO1	Use the fundamental concepts of cryptography.	
CO2	Design finite field arithmetic on FPGA.	
CO3	Implement efficient elliptic curve scalar multiplication on FPGAs	
CO4	Determine different side channel attacks.	
CO5	Develop Physically Unclonable Functions.	
REFERENCES:		
1.	Behrouz A. Forouzan and Debdeep Mukhopadhyay, "Introduction to Cryptography and Network Security", McGraw Hill,2018.	
2.	Debdeep Mukhopadhyay and Rajat Subhra Chakraborty, "Hardware Security: Design, Threats, and Safeguards", CRC Press, 2014.	
3.	Christian Wachsmann & Ahmad-Reza Sadeghi*,"* Physically Unclonable Functions (PUFs): Applications, Models, and Future Directions*",* Springer, 2015.	
4.	Bhunia, Swarup, and Mark M. Tehranipoor. "Hardware Security: A Hands-on Learning Approach". 1st ed., Academic Press, 2019.	
5.	Basel Halak," Physically Unclonable Functions" Springer / Academic Press, 2018.	
6.	Debdeep Mukhopadhyay and Rajat Subhra Chakraborty, *"*Hardware Security: Design, Threats, and Safeguards*"*, CRC Press, 2014.	

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	1	-	-	2	1	-
CO2	2	2	-	2	2	-
CO3	2	2	-	2	2	-
CO4	2	2	-	2	2	-
CO5	2	2	-	2	2	2
CO	2	2	-	2	2	1

VL22216	**PATTERN RECOGNITION**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**
COURSE OBJECTIVES:					
• To understand the fundamentals of Pattern recognition					
• To impart knowledge on various clustering techniques.					
• To study about feature extraction and selection.					
• To explore supervised machine learning methods.					
• To understand the artificial neural network.					
UNIT I	**PATTERN CLASSIFIER**				**9**
Overview of Pattern recognition – Discriminant functions – Supervised learning –Parametric estimation – Maximum Likelihood Estimation – Bayesian parameter Estimation – Problems with Bayes approach– Non Parametric techniques, Perceptron Algorithm-LMSE Algorithm- Pattern classification by distance functions – Minimum distance pattern classifier.					
UNIT II	**CLUSTERING**				**9**

Clustering Concept – Hierarchical Clustering Procedures – Partitional Clustering, Quick partitions- Mixture models - Sum-of-squares methods -k-nearest-neighbour method – Properties and Algorithms- Example application study -Clustering of Large Data Sets – EM Algorithm – Grid Based Clustering– Density Based Clustering.		
UNIT III	**FEATURE EXTRACTION AND SELECTION**	**9**
Entropy Minimization – KL Transforms – Regression-Linear, Non-linear and Logistic, Prediction, Feature Selection through Functions Approximation – Binary Feature Selection Feature selection criteria -Search algorithms for feature selection- Suboptimal search algorithms- Example application study.		
UNIT IV	**SUPERVISED MACHINE LEARNING METHODS**	**9**
Overview of machine learning- training–testing- Underfitting / Overfitting -Cross-Validation, Regression -Linear – Lasso - polynomial, Classification - Logistic Regression- Support Vector Machines –Kernel Methods, - Decision Trees.		
UNIT V	**ARTIFICIAL NEURAL NEWORK**	**9**
Supervised Learning - Unsupervised Learning- Reinforcement Learning – Feed Forward and Feedback architectures - Multilayer Perceptron - Back propagation Algorithm- Radial Basis Function networks - Introduction to Deep Learning– Convolution Neural Networks – Recurrent Neural Networks.		
		TOTAL: 45 PERIODS

COURSE OUTCOMES:	
Upon completion of the course, the students will be able to	
CO1	Apply neural networks for data preprocessing and feature extraction.
CO2	Analyze CNN architectures for object detection applications..
CO3	Analyze and compare transfer learning and recurrent neural network models..
CO4	Apply supervised machine learning techniques to evaluate predictive models.
CO5	Design and implement different neural network architectures for real-world problems.

REFERENCES:

1.	Josh Patterson and Adam Gibson “Deep Learning A Practitioner‘s A”, O‘Reilly Media, Inc.2017.
2.	Jojo Moolayil, “Learn Keras for Deep Neural Networks”, Apress,2018.
3.	Jose G. Delgado-Frias, William R. Moore, “VLSI for Artificial Intelligence and Neural Networks”, Springer Science Business Media, LLC, 2001
4.	Ibrahim M., Elfadel Duane S. Boning, and Xin Li, “Machine Learning in VLSI ComputerAided Design”. Springer, 2019.
5.	Mohamed I. Elmasry, “VLSI Artificial Neural Networks Engineering”, Springer Science Business Media, LLC, 2000
6.	E. S. Gopi, “Pattern Recognition and Computational Intelligence Techniques using Matlab”, Springer, 2019.

Mapping of Course Outcomes with Program Outcomes

Course Outcomes	**Programme Outcomes**					
	1	**2**	**3**	**4**	**5**	**6**
CO1	2	1	1	3	3	1
CO2	2	1	1	3	3	1
CO3	3	2	1	3	3	1
CO4	3	2	1	2	3	2
CO5	3	2	2	2	2	2
CO	3	2	1	3	3	1

SEMESTER II, PROFESSIONAL ELECTIVE – II

VL22221	**MIXED SIGNAL VLSI DESIGN**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:		
• To study the concepts of basic analog CMOS subcircuits and amplifiers.		
• To provide in-depth understanding of D/A and A/D converters.		
• To study the integrated circuits like PLLs and oscillators.		
• To learn the Analog and Digital layout design for mixed signal circuits.		
UNIT I	**BASIC ANALOG CMOS CIRCUITS**	**9**
Bias circuits in MOS Technology, MOS Current Mirrors and Current Sources, MOS Differential Amplifiers - Operational amplifiers: Single Stage Op-Amps, Two-stage Op-Amps, Fully Differential Op-Amps - Comparators: Single-Ended Auto-Zeroing Comparator, Differential Comparator, Differential comparator, Schmitt Trigger.		
UNIT II	**DIGITAL TO ANALOG CONVERTERS**	**9**
Fundamentals: Ideal D/A Converter, Quantization Noise, Deterministic Approach, Stochastic Approach – Decoder based converters: Resistor String Converters, Folded Resistor-String Converters – Binary-Scaled Converters: Binary Weighted Resistor Converters, Reduced-Resistance-Ratio Ladders, R-2R-Based Converters.		
UNIT III	**ANALOG TO DIGITAL CONVERTERS**	**9**
Ideal A/D Converter, Successive-Approximation Converters: DAC-Based Successive Approximation, Charge-Redistribution A/D, Resistor Capacitor Hybrid - Cyclic A/D Converter: Ratio-Independent Algorithmic Converter – Pipelined A/D Converter: One-Bit-Per-Stage Pipelined Converter, 1.5 Bit Per Stage Pipelined Converter, Flash Converter.		
UNIT IV	**PHASE LOCKED LOOPS**	**9**
Basic Phase-Locked Loop Architecture: Voltage Controlled Oscillator, Divider, Phase Detector, Loop Filer - Linearized Small-Signal Analysis: Second-Order PLL Model, Limitations of the Second- Order Small-Signal Model, PLL Design Example - Ring Oscillators, LC Oscillators, Phase Noise of Oscillators.		
UNIT V	**ANALOG AND DIGITAL LAYOUT DESIGN FOR MIXED SIGNAL**	**9**
Layout introduction: Introduction, MOS transistor layers, stick diagram, symbolic diagram - Digital layout design: Introduction, guide line of transistor layout, PMOS and NMOS transistor layout, CMOS transistor layout - Introduction to analog layout techniques and Passive component layout: Capacitor, Resistor and Inductor.		
		TOTAL: 45 PERIODS
COURSE OUTCOMES:		
Upon completion of the course, the students will be able to		
CO1	Explain the basic analog CMOS subcircuits and amplifiers.	
CO2	Develop different types of Digital to Analog Converters.	
CO3	Develop different types of Analog to Digital Converters.	
CO4	Design basic PLL circuits and oscillators.	
CO5	Design Layout for mixed signal model.	
REFERENCES:		
1.	P. Allen and D. Holberg, “CMOS Analog Circuit Design”, Oxford University Press, Second Edition, 2012.	
2.	B. Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, Second Edition, 2017.	
3.	R. Jacob Baker, H.W. Li and D.E. Boyce, “CMOS Circuit Design, Layout and Simulation”, Wiley Publishers, Fourth Edition, 2019.	
4.	David Johns, Tony Chan Carusone and Kenneth Martin, “Analog Integrated Circuit Design", Wiley, Second Edition, 2012.	
5.	Rui Paulo da Silva Martins and Pui-In Mak, “Analog and Mixed-Signal Circuits in Nanoscale CMOS”, Springer, 2024.	
6.	Yangyuan Wang, Min-Hwa Chi, Jesse Jen-Chung Lou, “Handbook of Integrated Circuit Industry”, Springer Nature, 2023.	

Mapping of Course Outcomes with Program Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**

CO1	1	-	2	2	1	-
CO2	1	-	2	2	1	-
CO3	1	-	2	2	1	-
CO4	1	-	2	2	1	-
CO5	1	-	2	2	1	-
CO	1	-	2	2	1	-

VL22222	**VLSI FOR WIRELESS COMMUNICATION**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To understand the concepts of basic wireless communication concepts.
- To study the Transmitter and receiver architectures of VLSI for wireless Communication.
- To understand the various types of mixers designed for wireless communication.
- To understand the application of frequency synthesizers.
- To study and design PLL and VCO.

UNIT I **OVERVIEW OF WIRELESS COMMUNICATION SYSTEMS** **9**

Overview of Wireless systems – Standards – Access Methods – Modulation schemes – Classical channel – Wireless channel description – Path loss – Multipath fading – Channel Model - Envelope Fading - Frequency Selective Fading – Fast Fading - Comparison of different types of Fading.

UNIT II **RECEIVER ARCHITECTURE** **9**

Receiver front end – Filter design – Band Selection Filter - Image Rejection Filter - Channel Filter - Non-idealities – Design parameters – Noise figure & Input intercept point. LNA Introduction – Wideband LNA design – Narrow band LNA design: Impedance matching & Core amplifier.

UNIT III **ACTIVE AND PASSIVE MIXER** **9**

Active Mixer: Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion – Noise - A Complete Active Mixer. Passive Mixer: Switching Mixer – Distortion, Conversion Gain & Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain, Distortion, Intrinsic & Extrinsic Noise in Single Ended Sampling Mixer.

UNIT IV **FREQUENCY SYNTHESIZERS** **9**

Phase Locked Loops - Voltage Controlled Oscillators - Phase Detector – Analog Phase Detectors – Digital Phase Detectors - Frequency Dividers - LC Oscillators - Ring Oscillators - Phase Noise - A Complete Synthesizer Design Example (DECT Application)

UNIT V **TRANSMITTER ARCHITECTURE** **9**

Transmitter back end design – Quadrature LO generator – Single ended RC and LC, R-C with Differential stages - Polyphase IQ generator - Divider based generator, Power Amplifier Design.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of the course, the students will be able to

CO1	Describe the basic wireless communication concepts.
CO2	Explain the parameters in receiver and a low noise amplifier.
CO3	Use appropriate mixer types in wireless communication applications.
CO4	Design the frequency synthesizers
CO5	Construct the transmitters and the power amplifiers for wireless communication.

REFERENCES:

1.	Thomas H.Lee, “The Design of CMOS Radio –Frequency Integrated Circuits’, Cambridge University Press, 2014.
2.	Emad N Farag, M.I Elmasry, “Mixed Signal VLSI Wireless Design Circuits and Systems”, Kluwer Publications, 2013.
3.	DALAL & UPENA, Wireless Communication, Oxford University Press, New Delhi, 2014.
4.	Bosco Leung, "VLSI for Wireless Communication, Second Edition, Springer publications, 2014.
5.	Wen-Chih Kan,“VLSI Architecture for High-capacity Wireless Communications”, University of Minnesota, 2007.

6.	David Tse and PramodViswanath, “Fundamentals of Wireless Communication”, Cambridge Press, 2005.

Mapping of Course Outcomes with Program Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	1	1	1	2	1	2
CO2	2	1	2	2	2	2
CO3	2	1	2	2	2	2
CO4	2	1	2	2	2	2
CO5	2	1	2	2	2	2
CO	2	1	2	2	2	2

VL22223	**RF IC Design**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To study the various impedance matching techniques used in RF circuit design.
- To understand the functional design aspects of LNAs, Mixers, PLLs and VCOs.
- To understand frequency synthesis.

UNIT I	**IMPEDANCE MATCHING IN AMPLIFIERS**	**9**

Definition of ‘Q’, Series Parallel Transformations of Lossy Circuits, Impedance Matching Using ‘L’, ‘Pi’ and T Networks, Integrated Inductors, Resistors, Capacitors, Tunable Inductors, Transformers.

UNIT II	**AMPLIFIER DESIGN**	**9**

Noise characteristics of MOS devices – thermal and flicker noise, Design of Common-Gate (CG) and Inductively Degenerated Common Source (CS) LNAs – input matching, gain, and noise optimization, Principles of RF Power Amplifier Design – efficiency, linearity, and output matching.

UNIT III	**ACTIVE AND PASSIVE MIXERS**	**9**

Qualitative Description of the Gilbert Mixer - Conversion Gain, and Distortion and Noise, Analysis of Gilbert Mixer, Switching Mixer - Distortion in Unbalanced Switching Mixer -Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - a Practical Unbalanced Switching Mixer, Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.

UNIT IV	**OSCILLATORS**	**9**

Design and operation of LC Oscillators, Voltage Controlled Oscillators (VCOs), and Ring Oscillators. Delay cell modeling and frequency control. Tuning mechanisms – tuning range in ring and LC oscillators, tuning sensitivity. Phase noise in oscillators – sources, modeling, and reduction techniques.

UNIT V	**PLL AND FREQUENCY SYNTHESIZERS**	**9**

Phase Detector/Charge Pump, Analog Phase Detectors, Digital Phase Detectors, Frequency Dividers, Loop Filter Design, Phase Locked Loops, Phase Noise in PLL, Loop Bandwidth, Basic Integer-N Frequency Synthesizer, Basic Fractional-N Frequency Synthesizer.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of the course, the students will be able to

CO1	Apply RF receiver front-end principles in wireless systems.
CO2	Design and apply constraints for LNAs, Mixers and frequency synthesizers.
CO3	Analyze and design mixers.
CO4	Design different types of oscillators and perform noise analysis.
CO5	Design PLL and frequency synthesizer.

REFERENCES:

1.	Robert Sobot - Wireless Communication Electronics: Introduction to RF Circuits and Design Techniques, 2nd Edition, 2021.
2.	Scott Kuzdeba - Radio Frequency Machine Learning: A Practical Deep Learning Perspective, Artech House Publishers, Unabridged Edition, 2025.
3.	Behzad Razavi – RF Microelectronics, 2nd Edition, Pearson Education, 2012.
4.	John W.M. Rogers & Calvin Plett – Radio Frequency Integrated Circuit Design, 2nd Edition, Artech House, 2010.
5.	Thomas H. Lee – The Design of CMOS Radio-Frequency Integrated Circuits, 2nd Edition, Cambridge University Press, 2004.
6.	Roland E. Best – Phase-Locked Loops: Design, Simulation, and Applications, 6th Edition, McGraw-Hill, 2007.

Mapping of Course Outcomes with Program Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	2	1	3	3	2	1
CO2	2	1	3	3	2	1
CO3	2	1	3	3	2	1
CO4	2	1	3	3	2	1
CO5	2	1	3	3	2	1
CO	2	1	3	3	2	1

VL22224	**EMBEDDED SYSTEM DESIGN**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To understand the design challenges in embedded systems.
- To program the Application Specific Instruction Set Processors.
- To understand the bus structures and protocols.
- To model processes using a state – machine model.
- To design a real time embedded system.

UNIT I	**EMBEDDED SYSTEM OVERVIEW**	**9**

Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Components, Optimizing Custom Single-Purpose Processors.

UNIT II	**GENERAL AND SINGLE PURPOSE PROCESSOR**	**9**

Basic Architecture, Pipelining, Superscalar and VLIW Architectures, Programmer's View, Development Environment, Application-Specific Instruction-Set Processors (ASIPS) Microcontrollers, Timers, Counters and Watchdog Timer, UART, LCD Controllers and Analog-to-Digital Converters, Memory Concepts.

UNIT III	**BUS STRUCTURES**	**9**

Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus - based I/O, Arbitration, Serial Protocols, I2C, CAN and USB, Parallel Protocols – PCI and ARM bus, Wireless Protocols – IRDA, Bluetooth, IEEE 802.11.

UNIT IV	**STATE MACHINE AND CONCURRENT PROCESS MODELS**	**9**

Basic State Machine Model, Finite-State Machine with Data path Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, RTOS – System design using RTOS.

UNIT V	**SYSTEM DESIGN**	**9**

Burglar alarm system-Design goals -Development strategy-Software development-Relevance to more complex designs- Need for emulation -Digital echo unit-Creating echo and reverb-Design requirements-Designing the codecs -The overall system design

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of the course, the students will be able to	
CO1	Explain and differentiate various communication protocols used in embedded systems.
CO2	Apply state machine techniques and design process models.
CO3	Apply knowledge of embedded software development tools and RTOS .
CO4	Apply networking principles in embedded devices.
CO5	Design suitable embedded systems for real world applications.
REFERENCES:	
1.	Frank Vahid and Tony Gwargie, "Embedded System Design", John Wiley & Sons, edition 3, 2018.
2.	Steve Heath, "Embedded System Design", Elsevier, Second Edition, 2004.
3.	Bruce Powel Douglas, "Real Time UML, Second Edition: Developing Efficient Objects for Embedded Systems", 3rd Edition 2004, Pearson Education
4.	Daniel W.Lewis, "Fundamentals of Embedded Software where C and Assembly Meet", Pearson Education, 2004
5.	Bruce Powel Douglas, "Real Time UML; Second Edition: Developing Efficient Objects for Embedded Systems", 3rd Edition 1999, Pearson Education.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	1	1	2	2	3	1
CO2	1	1	2	2	3	1
CO3	1	1	2	2	3	1
CO4	1	1	2	2	3	1
CO5	1	1	2	2	3	1
CO	1	1	2	2	3	1

VL22225	**POWER MANAGEMENT AND CLOCK DISTRIBUTION CIRCUITS**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To understand the principles of voltage and current reference circuits and their significance in analog integrated circuit design.
- To understand the fundamentals of oscillator and phase-locked loop operation, including stability and noise considerations.
- To apply the concepts of biasing and regulation to design low-dropout (LDO) voltage regulators with desired performance characteristics.
- To apply clock distribution and data recovery techniques to analyze and design timing circuits for high-speed communication systems.

UNIT I	**BIASING AND REFERENCE CIRCUIT DESIGN**	**9**

Current mirrors, self biased current reference, startup circuits, VBE based current reference, VT based current reference, band gap reference , supply independent biasing, temperature independent biasing, PTAT current generation, constant Gm biasing.

UNIT II	**LOW DROP OUT REGULATORS**	**9**

Analog building blocks, negative feedback, performance metrics, AC design, stability, internal and external compensation, PSRR – internal and external compensation circuits

UNIT III	**OSCILLATOR FUNDAMENTALS**	**9**

General considerations, ring oscillators, LC oscillators, Colpitts oscillator, jitter and phase noise in ring oscillators, impulse sensitivity function for LC & ring oscillators, phase noise in differential LC oscillators.

UNIT IV	**CLOCK DISTRIBUTION CIRCUITS**	**9**

PLL fundamental, PLL stability, noise performance, charge-pump PLL topology, CPPLL building blocks, jitter and phase noise performance, DLL fundamentals.		
UNIT V	**CLOCK AND DATA RECOVERY CIRCUITS**	**9**
CDR architectures, transimpedance amplifiers and limiters, CMOS interface, linear half rate CMOS CDR circuits, wide capture range CDR circuits.		
		TOTAL: 45 PERIODS

COURSE OUTCOMES:	
Upon completion of the course, the students will be able to	
CO1	Explain the operating principles and design considerations of bandgap reference circuits and low-dropout regulators
CO2	Interpret the specifications and performance parameters related to supply and clock generation circuits in integrated systems.
CO3	Choose suitable oscillator topologies and design them to meet specific clock generation requirements.
CO4	Design clock generation circuits for high-speed I/O interfaces, broadband communication, and data converter applications.
CO5	Implement clock distribution circuits to ensure timing accuracy and low jitter performance.

REFERENCES:	
1.	Amit Patra, Shailendra Baranwal, Ashis Maity, Samiran Dam, Syed Asif Eqbal , “Power Management Integrated Circuits: Architecture, Design and Implementation” ,CRC Press, 2024.
2.	Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Tata Mcgraw Hill, 2015.
3.	Gabriel.a. Rincon-Mora, “Analog IC Design with Low-Dropout Regulators”, Mcgraw-Hill Professional Pub, Second Edition 2014.
4.	Behzadrazavi, “Design of Integrated Circuits for Optical Communications”, McGraw Hill, Second Edition,2012.
5.	Floyd M. Gardner ,”Phase Lock Techniques” John Wiley& Sons, Inc 2005.
6.	Michiel Steyaert, Arthur H.M. Van Roermund, Herman Casier, “Analog Circuit Design: High Speed Clock and Data Recovery, High-Performance Amplifiers Power Management”,Springer, 2008.
7.	Gabriel.a. Rincon-Mora, "Voltage References from Diode to Precision Higher Order Band gap circuits”, John Wiley & Sons Inc, 2002.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	**Programme Outcomes**					
	1	**2**	**3**	**4**	**5**	**6**
CO1	1	1	2	2	2	1
CO2	1	1	2	2	2	1
CO3	1	1	2	2	2	1
CO4	1	1	2	2	2	1
CO5	1	1	2	2	2	1
CO	1	1	2	2	2	1

VL22226	**RECONFIGURABLE ARCHITECTURES**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To develop an overview and deeper insight that meets future needs of flexible processors.
- To learn the concepts of implementation, synthesis and placement of modules in reconfigurable architectures.
- To understand the communication techniques and System on Programmable Chip for reconfigurable architectures.
- To learn the process of reconfiguration management.
- To familiarize the applications of reconfigurable architectures.

UNIT I	INTRODUCTION	9
General purpose computing – domain specific processors – Application Specific Processors – reconfigurable computing –evolution of reconfigurable systems – simple Programmable Logic Devices – Complex Programmable Logic Devices – Field Programmable Gate Arrays – coarse grained reconfigurable devices.		
UNIT II	**IMPLEMENTATION, SYNTHESIS AND PLACEMENT**	**9**
Integration – FPGA design flow – logic synthesis – high level synthesis for reconfigurable devices– modelling – temporal partitioning algorithms – offline and online temporal placement – managing device's free space with empty rectangles and occupied spaces.		
UNIT III	**COMMUNICATION AND SOPC**	**9**
Direct communication – communication over third party – bus based communication – circuit switching – Network on Chip – dynamic Network on Chip – System on a Programmable Chip – adaptive multi-processing on chip.		
UNIT IV	**RECONFIGURATION MANAGEMENT**	**9**
Reconfiguration – configuration architectures – managing the reconfiguration process – reducing configuration transfer time – configuration security.		
UNIT V	**APPLICATIONS**	**9**
Pattern matching- video streaming - distributed arithmetic - adaptive controller- adaptive cryptographic systems- Software Defined Radio- High Performance Computing.		
		TOTAL: 45 PERIODS

COURSE OUTCOMES:	
Upon completion of the course, the students will be able to	
CO1	Implement appropriate architectural principles in the design of reconfigurable computing systems.
CO2	Implement appropriate trade-off decisions to satisfy area, power, and timing constraints in reconfigurable systems.
CO3	Implement placement and partitioning algorithms to achieve efficient resource utilization in reconfigurable architectures.
CO4	Apply communication techniques and system on programmable chip concepts to analyze reconfigurable architectures.
CO5	Apply the principles of network on chip and system on programmable chip in designing or evaluating reconfigurable systems.

REFERENCES:	
1.	Christophe Bobda, "Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications", Springer 2007.
2.	Scott Hauck and Andre Dehon, "Reconfigurable Computing: The Theory and Practice of FPGA Based Computation", Elsevier 2008.
3.	M. Gokhale and P. Graham, "Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays", Springer, 2005.
4.	Nikoloas Voros Et Al. "Applied Reconfigurable Computing: Architectures, Tools and Applications" Springer, 2023.
5.	Koen Bertels, João M.P. Cardoso, Stamatis Vassiliadis, "Reconfigurable Computing: Architectures and Applications", Springer 2006.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	1	1	2	1	1	-
CO2	2	-	2	2	1	-
CO3	1	1	2	1	1	-
CO4	1	-	2	1	1	-
CO5	1	1	2	1	1	-
CO	1	1	2	1	1	-

SEMESTER III, PROFESSIONAL ELECTIVES – III

VL22311	VLSI TESTING	L	T	P	C

		3	**0**	**0**	**3**
COURSE OBJECTIVES:					
• To familiarize with the basics of VLSI testing.					
• To explain logic and fault simulation along with testability measures.					
• To learn test generation techniques for combinational and sequential circuits.					
• To understand design for testability concepts.					
• To explore methods for fault diagnosis.					
UNIT I	**OVERVIEW OF TESTING**				**9**
VLSI Testing Process and Test Equipment – Challenges in VLSI Testing - Test Economics and Product Quality – Fault Modeling – Relationship Among Fault Models.					
UNIT II	**LOGIC & FAULT SIMULATION & TESTABILITY MEASURES**				**9**
Simulation for Design Verification and Test Evaluation – Modeling Circuits for Simulation – Algorithms for True Value and Fault Simulation – SCOAP Controllability and Observability.					
UNIT III	**TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS**				**9**
Algorithms and Representations – Redundancy Identification – Combinational ATPG Algorithms – Sequential ATPG Algorithms – Simulation Based ATPG – Genetic Algorithm Based ATPG.					
UNIT IV	**DESIGN FOR TESTABILITY**				**9**
Design for Testability Basics – Testability Analysis - Scan Cell Designs – Scan Architecture – Builtin Self-Test – Random Logic Bist – DFT for Other Test Objectives.					
UNIT V	**FAULT DIAGNOSIS**				**9**
Basic Definitions – Fault Models for Diagnosis – Generation of Vectors for Diagnosis – Combinational Logic Diagnosis - Scan Chain Diagnosis – Logic BIST Diagnosis.					
					TOTAL: 45 PERIODS
COURSE OUTCOMES:					
Upon completion of the course, the students will be able to					
CO1	Explain the VLSI testing process.				
CO2	Apply logic simulation and fault simulation techniques.				
CO3	Apply combinational and sequential ATPG algorithms to generate test vectors.				
CO4	Apply design-for-testability techniques including scan architectures and BIST.				
CO5	Apply fault diagnosis methods to identify defects in combinational logic, scan chains, and logic BIST.				
REFERENCES:					
1.	Michael L. Bushnell and Vishwani D. Agrawal, “Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2017.				
2.	Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, “VLSI Test Principles and Architectures”, Elsevier, 2017.				
3.	Niraj K. Jha and Sandeep Gupta, “Testing of Digital Systems”, Cambridge University Press, 2017.				
4.	Abhijit Joshi, “Digital Systems Testing and Testable Design”, Morgan Kaufmann, 2022.				
5.	Alex Krstic & Kenneth Leeb, “IC Testing: Next Generation Test Technology”, Springer, 2020.				
6.	Xiaoqing Wen, Kaoru Yamazaki, Kazuo Kinoshita, “Integrated Circuit Testing and Design-for-Testability”, Springer, 2018.				

Mapping of Course Outcomes with Program Outcomes

Course Outcomes	**Programme Outcomes**					
	1	**2**	**3**	**4**	**5**	**6**
CO1	2	1	2	3	3	1
CO2	2	1	2	2	3	1
CO3	1	1	2	2	3	1
CO4	1	1	2	3	2	1
CO5	2	1	2	2	1	1
CO	2	1	2	2	2	1

VL22312	SIGNAL INTEGRITY FOR HIGH SPEED DESIGN	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To introduce the principles of wave propagation, reflection and delay on transmission lines and microstrip/stripline structures.
- To understand coupling, cross-talk and methods to minimize interference in transmission systems.
- To explain the influence of parasitic elements, discontinuities and losses on signal integrity.
- To apply power integrity and decoupling design principles for high-speed systems using modeling tools.
- To apply timing and clock design techniques to ensure system synchronization and minimize jitter.

UNIT I **SIGNAL PROPAGATION ON TRANSMISSION LINES** **9**

Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams .Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching, input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion.

UNIT II **MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK** **9**

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossles models.

UNIT III **NON-IDEAL EFFECTS** **9**

Non-ideal signal return paths – gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses – Rs, tanδ , routing parasitic, Common-mode current, differential-mode current , Connectors.

UNIT IV **POWER CONSIDERATIONS AND SYSTEM DESIGN** **9**

SSN/SSO , DC power bus design , layer stack up, SMT decoupling , Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic ,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis.

UNIT V **CLOCK DISTRIBUTION AND CLOCK OSCILLATORS** **9**

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of the course, the students will be able to

CO1	Use signal propagation and reflection concepts to determine how signals behave on transmission lines.
CO2	Apply the concepts of cross-talk and coupling in multi-conductor lines and interpret the resulting impact on signal integrity.
CO3	Analyze the non-ideal effects and parasitic behaviors present in transmission systems.
CO4	Examine the role of power distribution and signal integrity design principles in the design process.
CO5	Inspect techniques for clock distribution and their impact on jitter performance.

REFERENCES:

1.	Douglas Brooks, “Signal Integrity Issues and Printed Circuit Board Design”, Prentice Hall Modern Semiconductor Design Series, 2012.
2.	Eric Bogatin , “Signal and Power Integrity – Simplified” , Pearson Modern Semiconductor Design Series , 2018.
3.	H. W. Johnson and M. Graham, “High-Speed Digital Design: A Handbook of Black Magic”, Pearson Education India, 2020.
4.	S. Hall, G. Hall, and J. McCall, “High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices”, Wiley-IEEE Press, 2008.
5.	Stephen C Thierauf, “High-Speed Circuit Board Signal Integrity”,Artech House,2017.

6.	James A. McCall ,Stephen H. Hall and Garrett W. Hall , "High -Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices", Wiley-IEEE Press,2014.

Mapping of Course Outcomes with Program Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	3	3	2	2	1	1
CO2	3	3	2	3	2	1
CO3	3	3	2	3	2	1
CO4	2	3	3	3	3	2
CO5	2	2	3	3	3	2
CO	3	3	2	3	2	1

VL22313	**VLSI SIGNAL PROCESSING**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To introduce techniques for altering existing DSP structures to suit VLSI implementations
- To introduce efficient design of DSP architectures suitable for VLSI

UNIT I	**OVERVIEW OF DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS**	**9**

Overview of DSP systems – typical DSP algorithms, data flow and dependence graphs – critical path, loop bound, iteration bound, longest path matrix algorithm, pipelining and parallel processing of FIR filters, pipelining and parallel processing for low power

UNIT II	**RETIMING, ALGORITHMIC STRENGTH REDUCTION**	**9**

Retiming – definitions and properties, unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even, Merge-Sort architecture, parallel rank-order filters.

UNIT III	**FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS**	**9**

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with powerof-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT IV	**BIT-LEVEL ARITHMETIC ARCHITECTURES**	**9**

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, design of lyon‟s bit-serial multipliers using Horner‟s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner‟s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT V	**NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS AND ASYNCHRONOUS PIPELINING**	**9**

Numerical strength reduction – sub-expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining - Bundled Data versus Dual-Rail protocol.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of the course, the students will be able to

CO1	Apply pipelining and parallel processing techniques to modify DSP algorithm dataflows and design efficient FIR filter architectures.
CO2	Analyse and modify the design equations leading to efficient DSP architectures for transforms apply low power techniques for low power dissipation.
CO3	Apply techniques to design fast convolution and IIR filter architectures.

CO4	Develop fast and area efficient multiplier architectures.
CO5	Apply numerical strength reduction and clocking strategies to build fast, low-power digital systems.

REFERENCES:

1.	Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and Implementation ", Wiley, Interscience, 2007.
2.	S. Salivahanan, A. Vallavaraj and C. Gnanapriya, "Digital Signal Processing", McGraw-Hill Education, 2nd Edition, 2018.
3.	Shankar B. Iyer and Sunil D. Sherlekar, "VLSI Synthesis of DSP Kernels: Algorithmic and Architectural Transformations", Springer, Reprint Edition, 2016.
4.	Durgesh Nandan, Ranjan Kumar Mohanty and Dinesh Kumar Arya, "VLSI Architecture for Signal, Speech and Image Processing", Apple Academic Press, CRC Press, 2023.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	3	2	2	2	2	-
CO2	3	2	2	2	2	-
CO3	3	-	2	-	2	2
CO4	3	-	2	-	2	-
CO5	3	-	2	-	2	2
CO	3	2	2	2	2	2

VL22314	**CAD FOR VLSI DESIGN**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To introduce the VLSI design methodologies and design methods.
- To introduce data structures and algorithms required for VLSI design.
- To study algorithms for partitioning and placement.
- To study algorithms for floor planning and routing.
- To study algorithms for modelling, simulation and synthesis.

UNIT I	**DESIGN METHODOLOGIES**	**9**

VLSI Design Methodologies – VLSI Design Cycle – New Trends in VLSI Design Cycle – Physical Design Cycle – New Trends in Physical Design Cycle – Design Styles – Review of VLSI Design Automation Tool.

UNIT II	**DATA STRUCTURES AND BASIC ALGORITHMS**	**9**

Overview of Data Structures and Algorithms – Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable Problems – General Purpose Methods for Combinatorial Optimization.

UNIT III	**ALGORITHMS FOR PARTITIONING AND PLACEMENT**	**9**

Layout Compaction – Problem Formulation – Algorithms for Constraint Graph Compaction – Partitioning – Placement – Placement Algorithms.

UNIT IV	**ALGORITHMS FOR FLOORPLANNING AND ROUTING**	**9**

Floorplanning – Problem Formulation – Floor planning Algorithms – Routing – Area Routing – Global Routing – Detailed Routing.

UNIT V	**MODELLING, SIMULATION AND SYNTHESIS**	**9**

Simulation – Gate Level Modeling and Simulation – Logic Synthesis and Verification – Binary Decision Diagrams – High Level Synthesis.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of the course, the students will be able to

CO1	Use various VLSI design methodologies.
CO2	Implement different data structures and algorithms required for VLSI design.
CO3	Execute algorithms for partitioning and placement.

CO4	Design algorithms for floor planning and routing.
CO5	Employ algorithms for modelling, simulation and synthesis.
REFERENCES:	
1.	Sabih H. Gerez, "Algorithms for VLSI Design Automation", Second Edition, Wiley-India, 2017.
2.	Naveed a. Sherwani, "Algorithms for VLSI Physical Design Automation", Third Edition, Springer, 2017.
3.	Brian Johnson, "Algorithms for VLSI Physical Design Automation", Intelliz Press, 2017.
4.	Charles J. Alpert, Dinesh P. Mehta and Sachin S Sapatnekar, "Handbook of Algorithms for Physical Design Automation, CRC Press, 2008.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	2	1	1	2	2	1
CO2	2	1	1	2	2	1
CO3	2	1	1	2	2	1
CO4	2	1	1	2	2	1
CO5	2	1	1	2	2	1
CO	2	1	1	2	2	1

VL22315	**SYSTEM-ON-CHIP**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- Introducing design, optimization, and programing a modern System-on-a-Chip.
- To understand the concepts of System on Chip Design methodology for Logic and Analog Cores.
- Making them understand about signal integrity aware SoC design and Scheduling algorithms.
- To understand the concepts of System on Chip Design Validation.
- To understand the concepts of SOC Testing.

UNIT I	**SYSTEM ON CHIP CONCEPTS**	**9**

System trade-offs and evolution of ASIC Technology- System on chip concepts and methodology– SoC design issues -SoC challenges and components.

UNIT II	**DESIGN METHODOLOGY FOR LOGIC CORES**	**9**

Design Methodological for Logic Cores- SoC Design Flow – On-chip buses –Design process for hard cores –Soft and firm cores – Core and SoC design examples.

UNIT III	**DESIGN METHODOLOGY FOR MEMORY ANALOG CORES**	**9**

Design Methodology for Memory and Analog Cores- Embedded memories –Simulation modes Specification of analog circuits – A to D converter –Phase locked loops –High I/O.

UNIT IV	**DESIGN VALIDATION**	**9**

Design Validation- Core level validation –Test benches –SoC design validation – Co simulation – hardware/ Software co-verification. Case Study: Validation and test of systems on chip.

UNIT V	**SYSTEM ON CHIP TESTING**	**9**

SoC Testing- SoC Test Issues –Cores with boundary scan –Test methodology for design reuse– Testing of microprocessor cores – Built in self-method –testing of embedded memories.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of the course, the students will be able to

CO1	Demonstrate an ability to identify, formulate and treat complex issues in the field of system-on-chip from a holistic perspective.
CO2	Apply SoC design methodologies to develop and optimize integrated systems comprising heterogeneous digital, analog, and mixed-signal components.
CO3	Design and evaluate various embedded memory architectures (such as SRAM, DRAM, ROM, and non-volatile memories) for performance, area, and power optimization in SoC applications.

CO4	Apply testing strategies and design validation techniques to ensure functional correctness, reliability, and manufacturability of SoC designs.
CO5	Develop and propose innovative techniques and solutions to address emerging challenges in future SoC and embedded system designs.

REFERENCES:

1.	Mark Keating, David Flynn, Robert Aitken, Alan Gibbons, Kaijian Shi, "Low Power Methodology Manual for System-on-Chip Design", Second Edition, Springer, 2017.
2.	Prakash Rashinkar, Peter Paterson, Leena Singh, "System-on-Chip Verification: Methodology and Techniques", Reprint Edition, Springer, 2016.
3.	Hoi-Jun Yoo, Kangmin Lee, Jun Kyoung Kim, "Low-Power NoC for High-Performance SoC Design", CRC Press, 2016.
4.	Michael J. Flynn, Wayne Luk, "Computer System Design: System-on-Chip", Wiley, 2017.
5.	Ahmed Amine Jerraya, Wayne Wolf, Grant Martin, "Multiprocessor Systems-on-Chips", Second Edition, Morgan Kaufmann, 2018.
6.	Krishnendu Chakrabarty, Erik Jan Marinissen, "SOC (System-on-Chip) Testing for Plug and Play Test Automation", Springer, 2016.

Mapping of Course Outcomes to Program Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	2	2	2	1	1	2
CO2	2	2	2	1	1	2
CO3	2	2	2	1	1	2
CO4	2	2	2	1	1	2
CO5	2	2	2	1	1	2
CO	2	2	2	1	1	2

VL22316	**NANO SCALE DEVICES**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To introduce novel MOSFET devices and understand the advantages of multi-gate devices.
- To learn the concepts of Multigate MOS systems.
- To know the various nano wire FETs.
- To learn the concepts of semiconductor nanodevices.
- To learn the concepts of Microfabrication and VLSI Technology.

UNIT I	**NOVEL MOSFETS**	**9**

MOSFET scaling, short channel effects, channel engineering, source/drain engineering, high-k dielectric, copper interconnects, strain engineering, SOI MOSFET, multigate transistors- single gate, double gate, triple gate and surround gate, quantum effects, volume inversion, threshold voltage, inter-subband scattering, multigate technology, carrier mobility, gate stack.

UNIT II	**PHYSICS OF MULTIGATE MOS SYSTEMS**	**9**

MOS Electrostatics,1D,2D, MOS Electrostatics, MOSFET Current-Voltage Characteristics, CMOS Technology, Ultimate limits, double gate MOS system, gate voltage effect, semiconductor thickness effect, asymmetry effect, oxide thickness effect, electron tunnel current, two- dimensional confinement, scattering.

UNIT III	**NANOWIRE FETS AND TRANSISTORS AT THE MOLECULAR SCALE**	**9**

Silicon nanowire MOSFETs, The I-V characteristics for nondegenerate and degenerate carrier statistics, Carbon nanotube, Band structure of carbon nanotube Band structure of grapheme, Physical structure of nanotube, Band structure of nanotube, Carbon nanotube FETs, Carbon nanotube MOSFETs, Schottky barrier carbon nanotube FETs, Electronic conduction in molecules, General model for ballistic nano transistors, MOSFETs with 0D, 1D, and 2D channels, Molecular transistors, Single electron charging, Single electron transistors.

UNIT IV	SEMICONDUCTOR NANODEVICES	9
Single Electron devices, Nano scale MOSFET, Resonant tunnelling transistor, Single electron transistors manipulation, Single electron dynamics, Mechanical Molecular Nano robotics, Nano devices and Nano computers: Theoretical models, Molecular devices, Micro and Optical Fibres, DNA based nano devices.		
UNIT V	**MICROFABRICATION AND VLSI TECHNOLOGY**	**9**
Microfabrication and VLSI Technology - Micro fabrication techniques, MEMS, Microfluidic devices, MOS transistor, NMOS, PMOS, CMOS, VLSI design issues, VLSI design techniques, Biosensors: Principles, DNA based biosensors, Protein based biosensors, Materials for biosensor applications, Fabrication of biosensors.		
		TOTAL: 45 PERIODS

COURSE OUTCOMES:	
Upon completion of the course, the students will be able to	
CO1	Interpret novel MOSFET devices and understand the advantages of multi-gate devices.
CO2	Analyze the underlying physical mechanisms governing the functional characteristics of multigate MOS systems.
CO3	Interpret Nanowire FETs and transistors at the molecular scale.
CO4	Apply basic principles to explain how semiconductor nanodevices work and where they are used.
CO5	Analyze micro fabrication and VLSI technologies to understand their impact on integrated system performance.

REFERENCES:	
1.	Khursheed Ahmad Shah, Farooq Ahmad Khanday, “Nanoscale Electronic Devices and Their Applications,” CRC Press, 2023.
2.	Mark Lundstrom, Jing Guo, “Nanoscale Transistors: Device Physics, Modeling and Simulation,” Springer, 2006.
3.	J. P. Colinge, “FINFETs and Other Multi-Gate Transistors,” Springer, 2008.
4.	M. S. Lundstrom, “Fundamentals of Carrier Transport,” 2nd Edition, Cambridge University Press, 2000.
5.	Mark Lundstrom, Jing Guo, "Nanoscale Transistors: Device Physics, Modeling and Simulation", Springer, 2006

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	3	1	3	2	1	2
CO2	3	1	3	2	1	2
CO3	3	1	3	2	1	2
CO4	3	1	3	2	1	2
CO5	3	1	3	2	1	2
CO	3	1	3	2	1	2

SEMESTER III, PROFESSIONAL ELECTIVES - IV

VL22321	PHYSICAL DESIGN AUTOMATION	L	T	P	C
		3	0	2	4

COURSE OBJECTIVES:
• To understand the concepts of physical design process such as partitioning, floor planning, placement and routing.
• To discuss the concepts of design optimization algorithms and their application to physical design automation.
• To understand the concepts of simulation and synthesis in VLSI design automation.
• To formulate CAD design problems using algorithmic methods.

UNIT I	**PHYSICAL DESIGN**	**9**
Layout and Design Rules, Materials for VLSI Fabrication, Basic Algorithmic Concepts for Physical Design, Physical Design Processes and Complexities. Partition: Kernigham-Lin’s Algorithm, Fiduccia Mattheyes Algorithm, Krishnamurthy Extension, Hmetis Algorithm, Multilevel Partition Techniques.		

UNIT II	FLOOR-PLANNING	9
Planning: Hierarchical Design, Wire Length Estimation, Slicing and Non-Slicing Floor Plan, Polar Graph Representation, Operator Concept, Stockmeyer Algorithm for Floor Planning, Mixed Integer Linear Program		
UNIT III	**PLACEMENT**	**9**
Design Types: ASICS, SOC, Microprocessor RLM; Placement Techniques: Simulated Annealing, Partition Based, Analytical, and Hall's Quadratic; Timing and Congestion Considerations.		
UNIT IV	**ROUTING**	**9**
Detailed, Global and Specialized Routing, Channel Ordering, Channel Routing Problems and Constraint Graphs, Routing Algorithms, Yoshimura And Kuh's Method, Zone Scanning and Net Merging, Boundary Terminal Problem, Minimum Density Spanning Forest Problem, Topological Routing, Cluster Graph Representation		
UNIT V	**SEQUENTIAL LOGIC OPTIMIZATION AND CELL BINDING**	**9**
State Based Optimization, State Minimization, Algorithms; Library Binding and Its Algorithms, Concurrent Binding.		
		45 PERIODS

PRACTICAL EXERCISES:	**30 PERIODS**
Experiments based on Verilog HDL/System Verilog	
1.	Graph Algorithms: Graph Search Algorithms, Spanning Tree Algorithm and Shortest Path Algorithm
2.	Partitioning Algorithms: Group Migration Algorithms, Simulated Annealing and Evolution Algorithms, Metric Allocation Method
3.	Floor Planning Algorithms: Constraint Based Methods, Integer Programming Based Method and Hierarchical Tree Based Methods
4.	Routing Algorithms: Two Terminal Algorithms and Multi Terminal Algorithm
	TOTAL:75 PERIODS

COURSE OUTCOMES:	
Upon completion of the course, the students will be able to	
CO1	Explain the fundamentals of VLSI physical design and partitioning algorithms.
CO2	Illustrate floorplanning techniques for hierarchical and optimized layout design.
CO3	Utilize placement methods considering timing and congestion constraints.
CO4	Develop routing algorithms to establish effective interconnections in complex VLSI circuits.
CO5	Utilize sequential logic optimization and cell binding techniques for efficient circuit implementation.

REFERENCES:

1.	Andrew B. Kahng, Jens Lienig Igor L. Markov, Jin Hu, "VLSI Physical Design: From Graph Partitioning to Timing Closure, 2nd Edition, 2022, Springer.
2.	Veena S. Chakravarthi, Shivananda R. Koteshwar,"SoC Physical Design: A Comprehensive Guide" 2022,Springer.
3.	Sherwani, "Algorithms for VLSI Physical Design Automation", 3rd Edition, 2013, Kluwer.
4.	Wolf. W, " Modern VLSI Design: IP-Based Design", 4th Ed., 2009, Pearson Education.
5.	Dreschler, "Evolutionary Algorithms for VLSI CAD ", 3rd Edition, 2010, Springer.
6.	Sait, S.M, And Youssef, "VLSI Physical Design Automation: Theory And Practice", 1999, World Scientific Publishing Company.

Mapping of Course Outcomes with Program Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	1	1	1	1	1	1
CO2	1	1	2	2	2	1
CO3	1	1	2	2	2	1
CO4	1	1	2	2	2	1
CO5	1	1	2	2	2	1
CO	1	1	2	2	2	1

V L22322	SYSTEM VERILOG	L	T	P	C
		3	0	2	4

COURSE OBJECTIVES:

- Insight to apply system verilog concepts to do synthesis, analysis and architecture design.
- To master the usage of SystemVerilog data types, dynamic memory structures, and procedural routines for efficient hardware modeling.
- To apply Object-Oriented Programming principles, such as classes, inheritance, and encapsulation, to build modular and reusable verification environments.
- To implement concurrent execution using threads and inter-process communication tools while measuring verification progress through functional coverage.
- To develop a complete, integrated SystemVerilog testbench using virtual interfaces to connect verification components to complex design blocks.

UNIT I	VERIFICATION METHODOLOGY	9

Verification Guidelines: Introduction, Verification Process, Verification Plan, Verification Methodology Manual, Basic Testbench Functionality, Directed Testing, Methodology Basics, Constrained-Random Stimulus, Functional Coverage, Testbench Components, Layered Testbench.

UNIT II	SYSTEM VERILOG BASICS AND CONCEPTS	9

Data Types: Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Creating New Types with Typedef, Creating User-Defined Structures, Enumerated Types, Constants, Strings. Procedural Statements and Routines: Procedural Statements, Tasks, Functions, and Void Functions.

UNIT III	OBJECT-ORIENTED PROGRAMMING (OOPS)	9

Where to Define a Class- OOPS Terminology -Creating New Objects -Object Deallocation- Using Objects -Static Variables Vs. Global Variables -Class Routines -Defining Routines Outside of The Class - Scoping Rules -Using One Class Inside Another - Understanding Dynamic Objects -Copying Objects -Public Vs. Private -Straying Off Course - Building a Testbench.

UNIT IV	THREADS AND INTER-PROCESS COMMUNICATION AND FUNCTIONAL COVERAGE	9

Working With Threads, Inter-Process Communication, Events, Semaphores, Mailboxes, Building a Testbench with Threads and IPC. Coverage Types, Functional Coverage Strategies, Simple Functional Coverage Example, Coverage Options, Parameterized Cover Groups, Analysing Coverage Data, Measuring Coverage Statistics.

UNIT V	A COMPLETE DSYSTEM VERILOG TESTBENCH AND ADVANCED INTERFACES	9

Design Blocks, Testbench Blocks, Alternate Tests, Virtual Interface with the ATM Router, Connecting to Multiple Design Configurations, Parameterized Interfaces and Virtual Interfaces, Procedural Code in an Interface.

45 PERIODS

PRACTICAL EXERCISES: 30 PERIODS

Experiments based on Verilog HDL/System Verilog

1.	Design a Testbench for 2x1 Mux Using Gates.
2.	Implementation of a Mailbox by Allocating Memory.
3.	Implementation and Testing of Semaphore for a Simple DUT.
4.	Implementation of Scoreboard for a Simple DUT.

TOTAL:75 PERIODS

COURSE OUTCOMES:

Upon completion of the course, the students will be able to

CO1	Apply verification principles and the layered testbench architecture to develop structured verification plans for complex digital designs.
CO2	Demonstrate the use of SystemVerilog's advanced data types and procedural routines to manage dynamic data during simulation.
CO3	Construct reusable and modular verification components by applying Object-Oriented Programming (OOP) techniques.
CO4	Implement concurrent testbench execution using threads and IPC mechanisms while validating design features through functional coverage metrics.
CO5	Develop a complete, scalable SystemVerilog testbench using virtual interfaces to verify

	communication between a design-under-test and its environment.
REFERENCES:	
1.	Chris Spear, Greg Tumbush "System Verilog for Verification: a Guide to Learning the Testbench Language Features", Springer, Third Edition, 2012.
2.	Ashok B Mehta, "Introduction to System Verilog" Springer, 2021.
3.	Chris Spear, "System Verilog for Verification: a Guide to Learning the Testbench Language Features", Springer 2006.
4.	Batra,"Digital Hardware Modelling Using SystemVerilog", PHI Learning, 2021.
5.	Mark Glasser, "Open Verification Methodology Cookbook", Springer, 2009.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	2	1	2	2	2	1
CO2	2	1	2	2	2	1
CO3	2	1	2	2	2	1
CO4	2	1	2	2	2	1
CO5	2	1	2	2	2	1
CO	2	1	2	2	2	1

VL22323	**DIGITAL IMAGING AND VIDEO PROCESSING**	**L**	**T**	**P**	**C**
		3	**0**	**2**	**4**

COURSE OBJECTIVES:

- To learn the basic understanding of image fundamentals and transforms
- To interpret the basic concepts of frequency domain filtering for image smoothing and sharpening.
- To demonstrate the use of boundary and regional descriptors for pattern recognition.
- To implement video signal formation and basic processing techniques in digital video systems.
- To explore motion estimation methods and their applications in video coding and compression.

UNIT I	**FUNDAMENTALS OF IMAGE PROCESSING AND TRANSFORMS**	**9**

Image sampling, Quantization, Resolution, Image file formats, Elements of image processing system, Need for transform, image transforms, Fourier transform, 2 D Discrete Fourier transform, Walsh transform, Hadamard transform, Haar transform, KL transform, singular value decomposition, Radon transform, comparison of different image transforms.

UNIT II	**ENHANCEMENT AND RESTORATION**	**9**

Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters. Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, Introduction to Image restoration, Image degradation, Image restoration model.

UNIT III	**SEGMENTATION AND RECOGNITION**	**9**

Edge detection, Edge linking via Hough transform – Thresholding – Region based segmentation – Region growing – Region splitting and merging – Morphological processing- erosion and dilation, Boundary representation, Boundary description, Fourier Descriptor, Regional Descriptors – Topological feature, Texture – Patterns and Pattern classes – Recognition based on matching.

UNIT IV	**BASIC STEPS OF VIDEO PROCESSING**	**9**

Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations

UNIT V	**2-D MOTION ESTIMATION**	**9**

Optical flow, optical flow constraints, General Methodologies, Pixel Based Motion Estimation, Block Matching Algorithm, Global Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

	45 PERIODS
PRACTICAL EXERCISES:	**30 PERIODS**
1.	Histogram Equalization
2.	Image Filtering (spatial-domain)
3.	Image Filtering (frequency-domain)
4.	Image Segmentation
5.	Familiarization with Video Processing tools
6.	Denoising video
7.	Video resizing
8.	Background subtraction
9.	Interpolation methods for re-sampling
10	Video encoding
	TOTAL:75 PERIODS
COURSE OUTCOMES:	
Upon completion of the course, the students will be able to	
CO1	Explain the fundamental concepts of image formation, quantization, resolution, and various image transforms.
CO2	Describe the spatial and frequency domain techniques for image enhancement and restoration.
CO3	Utilize the principles of segmentation, morphological operations, and feature extraction for image recognition.
CO4	Demonstrate the steps involved in video signal formation, sampling, and filtering operations in digital video systems.
CO5	Apply motion estimation methods for video coding and compression applications.
REFERENCES:	
1.	Gonzalez and Woods, “Digital Image Processing”, 3rd edition., Pearson, 2016.
2.	A L Bovik, “Handbook of Image and Video processing”, Academic press, 2010.
3.	K.R.Castelman, “Digital Image processing”, Prentice Hall, 1996.
4.	Anil Kumar Jain, “Fundamentals of Digital Image Processing”, Prentice Hall of India. Second edition, 2002.
5.	R C Gonzalez, R E Woods and S L Eddins, “Digital Image Processing Using Matlab”, Pearson Education , 2006.
6.	A. Murat Tekalp, “Digital Video Processing”, Prentice Hall Signal Processing, Second edition, 2015.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	**Programme Outcomes**					
	1	**2**	**3**	**4**	**5**	**6**
CO1	2	2	2	1	1	-
CO2	2	2	3	2	1	-
CO3	2	1	2	2	1	1
CO4	3	2	2	2	2	1
CO5	3	3	3	2	2	1
CO	2	2	2	2	1	1

MX22313	**DEEP LEARNING**	**L**	**T**	**P**	**C**
		3	**0**	**2**	**4**
COURSE OBJECTIVES:					
• To develop and Train Deep Neural Networks.					
• To develop a CNN for object detection and recognition.					
• To build and train RNNs, to solve real-world problems.					
• To study the structure of LSTM and GRU and the differences between them					

- To design Auto Encoders for Image Processing.

UNIT I	OVERVIEW OF DEEP LEARNING	9

Review of Neural Networks- Building Blocks of Neural Network. Multilayer Perceptron, Back propagation algorithm and its variants Stochastic gradient decent, Optimizers. Activation Functions. Loss Functions, Data Pre-processing for neural networks, Overfitting and Underfitting. Hyperparameters, Deep networks.

UNIT II	CONVOLUTIONAL NEURAL NETWORK	9

CNN. Architecture- Input Layers, Convolution Layers. Pooling Layers. Dense Layers, Filters and Feature Maps, Dropout Layers and Regularization, Batch Normalization. Various Activation Functions. Various Optimizers. Popular CNN Architectures: LeNet, AlexNet, VGG16, ResNet, UNet.

UNIT III	TRANSFER LEARNING & SEQUENCE MODELLING	9

Transfer Learning with Image Data. RCNN, Fast R-CNN, Faster R-CNN, Mask-RCNN, YOLO. Recurrent Neural Networks, Bidirectional RNNs (BRNN). Long Short-Term Memory (LSTM). Bi-directional LSTM. Sequence-to-Sequence Models (Seq2Seq). Gated recurrent unit GRU.

UNIT IV	DEEP REINFORCEMENT & UNSUPERVISED LEARNING	9

About Deep Reinforcement Learning. Q-Learning. Deep Q-Network (DQN). Policy Gradient Methods. Actor-Critic Algorithm. About Autoencoding. Convolutional Auto Encoding. Variational Auto Encoding. Generative Adversarial Networks.

UNIT V	APPLICATIONS OF DEEP LEARNING	9

Autoencoders for Feature Extraction. Auto Encoders for Classification. Denoising Autoencoders. Sparse Autoencoders. Case studies-Deep Neural network for Medical image segmentation.

45 PERIODS

PRACTICAL EXERCISES: 30 PERIODS

1.	Implement a perceptron in TensorFlow/Keras Environment.
2.	Implement a Feed-Forward Network in TensorFlow/Keras. for signal / Image data.
3.	Implement an Image Classifier using CNN in TensorFlow/Keras for abnormal detection.
4.	Implement a Transfer Learning concept for medical Image Classification.
5.	Implement an Autoencoder in TensorFlow/Keras and improve the deep learning model by tuning hyper parameters
6.	Implement a Simple LSTM using TensorFlow/Keras
7.	Implement a classifier in Recurrent Neural network.

TOTAL:75 PERIODS

COURSE OUTCOMES:

Upon completion of the course, the students will be able to

CO1	Realize neural network for data preprocessing and feature extraction.
CO2	Understand CNN architecture for object detection.
CO3	Understand transfer learning and recurrent networks.
CO4	Analyze the Deep Reinforcement & Unsupervised Learning networks
CO5	Apply deep learning network for Feature Extraction and Classification

REFERENCES:

1.	Josh Patterson and Adam Gibson, “Deep Learning A Practitioner‘s Approach”, O‘Reilly Media, Inc.2017.
2.	Jojo Moolayil, “Learn Keras for Deep Neural Networks”, Apress,2018..
3.	Santanu Pattanayak, “Pro Deep Learning with Tensor Flow”, Apress,2017.
4.	Vinita Silaparasetty, “Deep Learning Projects Using Tensor Flow 2”, Apress, 2020.
5.	Francois Chollet, “Deep Learning with Python”, Manning Shelter Island,2017.
6.	Ian Goodfellow, YoshuaBengio and Aaron Courville, “Deep Learning”, MIT Press, 2017..
7.	Umberto Michelucci, “Applied Deep Learning. A Case-based Approach to Understanding Deep Neural Networks”, Apress, 2018.
8.	https://nptel.ac.in/courses/106106184

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	1	1	-	-	2	1
CO2	1	1	-	1	2	1
CO3	1	1	-	1	2	1
CO4	1	1	-	2	2	1

CO5	1	1	-	2	2	1
CO	1	1	-	2	2	1

VL22324	**PCB DESIGN**	**L**	**T**	**P**	**C**
		3	**0**	**2**	**4**

COURSE OBJECTIVES:

- To understand the need for PCB Design and the types of PCBs.
- To understand the PCB Layout and Routing.
- To understand the various technology trends in PCB design.
- To understand the fabrication process of PCB.
- To understand the PCB production process.

UNIT I	**OVERVIEW OF PCB DESIGN**	**9**

Fundamental electronic components, electronic circuits, Need for PCB, Types of PCBs: Single and Multilayer, PCB Material, Electronic Component packaging.

UNIT II	**PCB LAYOUT AND ROUTING**	**9**

Layout planning, general rules and parameters, ground conductor considerations, thermal issues, check and inspection of artwork. PCB layout guidelines: trace width, spacing, ground planes, power planes, and thermal considerations, Routing techniques: manual and auto-routing.

UNIT III	**PCB TECHNOLOGY TRENDS**	**9**

Multilayer PCBs - Multiwire PCB, Flexible PCBs, Surface mount PCBs, Reflow soldering, Introduction to High-Density Interconnection (HDI) Technology.

UNIT IV	**PCB FABRICATION PROCESS AND ASSEMBLY**	**9**

Overview of fabrication steps: etching, drilling, plating, and solder masking, Assembly Techniques: Plated Through Hole, Surface Mount.

UNIT V	**PCB PROTOTYPING AND PRODUCTION**	**9**

PCB Prototyping: Photo-Lithography process, Screen Printing process and chemical etching. PCB Mass Manufacturing Process: Gerber Generation, CAM, PCB testing.

45 PERIODS

PRACTICAL EXERCISES: 30 PERIODS

Experiments based on KiCAD/ORCAD/CADENCE / Mentor Graphics

1.	PCB Design of Astable multivibrator.
2.	PCB Design of simple Power Supply
3.	PCB Design of IR sensor module
4.	PCB Design of Bridge rectifier
5.	PCB Design of PWM generator

COURSE OUTCOMES:

Upon completion of the course, the students will be able to

CO1	Explain the need for PCB design and the types of PCBs.
CO2	Explain the PCB design process.
CO3	Implement PCB technology trends such as multilayer, flexible, and HDI PCBs.
CO4	Execute PCB fabrication processes and utilize appropriate assembly techniques for electronic systems
CO5	Construct the PCB production process.

TOTAL:75 PERIODS

REFERENCES:

1.	Clyde F. Coombs, Jr, Happy T. Holden, “Printed Circuits Handbook”, Sixth edition, McGraw-Hill Professional, 2016.
2.	R. S. Khandpur,” Printed circuit board design, fabrication assembly and testing”, Tata McGraw Hill, 2017.
3.	Cezar Rigo,” Essentials of PCB Design: An Introductory Guide to Printed Circuit Board Engineering”, Kindle edition 2023.
4.	Simon Monk, “Make Your Own PCBs with EAGLE: From Schematic Designs to Finished Boards”, Second Edition, McGraw-Hill Education, 2017.

5.	Roger Hu,"PCB Design and Layout Fundamentals for EMC", 2019.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	2	1	1	1	2	1
CO2	2	1	1	1	2	1
CO3	2	1	1	1	2	1
CO4	2	1	1	1	2	1
CO5	2	1	1	1	2	1
CO	2	1	1	1	2	1

VL22325	**ADAPTIVE SIGNAL PROCESSING**	**L**	**T**	**P**	**C**
		3	**0**	**2**	**4**

COURSE OBJECTIVES:

- To understand the basic principles of discrete random signal processing.
- To understand the principles of spectral estimation.
- To learn about the weiner and adaptive filters
- To understand the different signal detection and estimation methods.
- To acquire skills to design synchronization methods for proper functioning of the system.

UNIT I	**DISCRETE RANDOM SIGNAL PROCESSING**	**9**

Discrete Random Processes, Random Variables, Parseval's Theorem, Wiener-Khintchine Relation, Power Spectral Density, Spectral Factorization, Filtering Random Processes, Special Types of Random Processes.

UNIT II	**SPECTRAL ESTIMATION**	**9**

Nonparametric Methods – Periodogram, Modified Periodogram, Bartlett, Welch and Blackman-Tukey Methods, Parametric Methods – ARMA, AR and MA Model Based Spectral Estimation, Solution Using Levinson-Durbin Algorithm.

UNIT III	**WEINER AND ADAPTIVE FILTERS**	**9**

Weiner Filter: FIR Wiener Filter, IIR Wiener Filter, Adaptive Filter: FIR Adaptive Filters – Steepest Descent Method- LMS Algorithm, RLS Adaptive Algorithm, Applications.

UNIT IV	**DETECTION AND ESTIMATION**	**9**

Bayes Detection Techniques, Map, Ml,– Detection of M-Ary Signals, Neymanpearson, Minimax Decision Criteria. Kalman Filter- Discrete Kalman Filter, The Extended Kalman Filter, Application.

UNIT V	**SYNCHRONIZATION**	**9**

Signal Parameter Estimation, Carrier Phase Estimation, Symbol Timing Estimator, Joint Estimation of Carrier Phase and Symbol Timing.

TOTAL: 45 PERIODS

PRACTICAL EXERCISES: 30 PERIODS

1.	Design of Non- Parametric and Parametric for Spectral Estimation
2.	Design of Linear Prediction Filter Using Matlab
3.	Design of LMS Filter Using Matlab
4.	Design of RLS Filter Using Matlab
5.	Design of Extended Kalman Filter Using Matlab

COURSE OUTCOMES:

Upon completion of the course, the students will be able to

CO1	Explain the basic principles of discrete random signal processing.
CO2	Discuss the principles of spectral estimation.
CO3	Design the Weiner and Adaptive filters.
CO4	Apply different signal detection and estimation methods.
CO5	Design the synchronization methods for proper functioning of the system.

REFERENCES:

1.	Monson H. Hayes, “Statistical Digital Signal Processing and Modeling”, John Wiley and Sons, Inc, Singapore, 2009.
2.	John G. Proakis., “Digital Communication”, 4th Edition, McGraw Hill Publications, 2001.
3.	Simon Haykin, “Adaptive Filter Theory”, Pearson Education, Fourth Edition, 2003
4.	Bernard Sklar and Pabitra Kumar Roy, “Digital Communications: Fundamentals and Applications”, 2/E, Pearson Education India, 2009
5.	Paulo S. R. Diniz, “Adaptive Filtering Algorithms and Practical Implementation”, Springer, 2011.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	1	-	1	1	1	1
CO2	1	1	2	1	1	1
CO3	2	-	2	1	1	1
CO4	2	-	1	1	1	1
CO5	2	1	2	2	1	1
CO	2	1	2	1	1	1

AUDIT COURSES

AC22101	**ENGLISH FOR RESEARCH PAPER WRITING**	**L**	**T**	**P**	**C**
		2	**0**	**0**	**0**

COURSE OBJECTIVES:

- Teach how to improve writing skills and level of readability
- Tell about what to write in each section
- Summarize the skills needed when writing a Title
- Infer the skills needed when writing the Conclusion
- Ensure the quality of paper at very first-time submission

UNIT I	**INTRODUCTION TO RESEARCH PAPER WRITING**	**6**

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT II	**PRESENTATION SKILLS**	**6**

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction.

UNIT III	**TITLE WRITING SKILLS**	**6**

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT IV	**RESULT WRITING SKILLS**	**6**

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions.

UNIT V	**VERIFICATION SKILLS**	**6**

Useful phrases, checking Plagiarism, how to ensure paper is as good as it could possibly be the first-time submission.

TOTAL: 30 PERIODS

COURSE OUTCOMES:

Upon completion of the course, the students will be able to

CO1	Understand that how to improve your writing skills and level of readability
CO2	Learn about what to write in each section
CO3	Understand the skills needed when writing a Title
CO4	Understand the skills needed when writing the Conclusion

CO5	Ensure the good quality of paper at very first-time submission
REFERENCES:	
1	Adrian Wallwork ," English for Writing Research Papers", Springer New York Dordrecht Heidelberg London, 2011
2	Day R, " How to Write and Publish a Scientific Paper", Cambridge University Press 2006
3	Goldbort R, "Writing for Science", Yale University Press (available on Google Books) 2006
4	Highman N, "Handbook of Writing for the Mathematical Sciences", SIAM. Highman's book 1998

Mapping of Course Outcomes with Program Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	-	2	-	1	-	-
CO2	-	2	-	1	-	-
CO3	-	2	-	1	-	-
CO4	-	2	-	1	-	-
CO5	-	2	-	1	-	-
CO	-	2	-	1	-	-

AC22102	**CONSTITUTION OF INDIA**	**L**	**T**	**P**	**C**
		2	**0**	**0**	**0**

COURSE OBJECTIVES:

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional
- Role and entitlement to civil and economic rights as well as the emergence nation hood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolutionin1917and its impact on the initial drafting of the Indian Constitution.
- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.

UNIT I	**HISTORY OF MAKING OF THE INDIAN CONSTITUTION**	**6**
History, Drafting Committee, (Composition & Working)		
UNIT II	**PHILOSOPHY OF THE INDIAN CONSTITUTION**	**6**
Preamble, Salient Features.		
UNIT III	**CONTOURS OF CONSTITUTIONAL RIGHTS AND DUTIES**	**6**
Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.		
UNIT IV	**ORGANS OF GOVERNANCE**	**6**
Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.		
UNIT V	**LOCAL ADMINISTRATION**	**6**
District's Admini of Elected Representative, CEO, Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy(Different departments), Village level:Role of Elected and Appointed officials, Importance of grass root democracy.		

UNIT VI	ELECTION COMMISSION	6
Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners - Institute and Bodies for the welfare of SC/ST/OBC and women.		
		TOTAL: 30 PERIODS

COURSE OUTCOMES:	
Upon completion of the course, the students will be able to	
CO1	Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
CO2	Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
CO3	Discuss the circumstances surrounding the foundation of the Congress Socialist Party[CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
CO4	Discuss the passage of the Hindu Code Bill of 1956.
CO5	Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.

REFERENCES:	
1	The Constitution of India,1950(Bare Act),Government Publication.
2	Dr.S.N.Busi, Dr.B. R.Ambedkar framing of Indian Constitution,First Edition, 2015.
3	M.P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis,2014.
4	D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

Mapping of Course Outcomes with Program Outcomes

Course Outcomes	Programme Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
CO1	-	2	1	-	-	-
CO2	-	2	1	-	-	-
CO3	-	2	1	-	-	-
CO4	-	2	1	-	-	-
CO5	-	2	1	-	-	-
CO	-	2	1	-	-	-

AC22201	**DISASTER MANAGEMENT**	**L**	**T**	**P**	**C**
		2	**0**	**0**	**0**

COURSE OBJECTIVES:
• Summarize basics of disaster
• Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
• Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
• Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
• Develop the strengths and weaknesses of disaster management approaches

UNIT I	OVERVIEW OF DISASTER	6
Disaster: Definition, Factors and Significance; Difference between Hazard And Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.		
UNIT II	**REPERCUSSIONS OF DISASTERS AND HAZARDS**	**6**
Economic Damage, Loss of Human and Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.		
UNIT III	**DISASTER PRONE AREAS IN INDIA**	**6**

Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides And Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference To Tsunami; Post-Disaster Diseases and Epidemics.		
UNIT IV	**DISASTER PREPAREDNESS AND MANAGEMENT**	**6**
Preparedness: Monitoring Of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological And Other Agencies, Media Reports: Governmental and Community Preparedness.		
UNIT V	**RISK ASSESSMENT**	**6**
Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.		
		TOTAL: 30 PERIODS

COURSE OUTCOMES:	
Upon completion of the course, the students will be able to	
CO1	Summarize basics of disaster
CO2	Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
CO3	Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
CO4	Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
CO5	Develop the strengths and weaknesses of disaster management approaches.

REFERENCES:	
1	Goel S. L., Disaster Administration And Management Text and Case Studies", Deep & Deep Publication Pvt. Ltd., New Delhi, 2009.
2	NishithaRai, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'NewRoyal book Company, 2007.
3	Sahni, Pardeep et.Al. ," Disaster Mitigation Experiences and Reflections", Prentice Hall OfIndia, New Delhi, 2001.
4	Goel S. L., Disaster Administration And Management Text and Case Studies", Deep & Deep Publication Pvt. Ltd., New Delhi,2009.

Mapping of Course Outcomes with Program Outcomes

Course Outcomes	**Programme Outcomes**					
	1	**2**	**3**	**4**	**5**	**6**
CO1	1	-	-	-	1	2
CO2	1	-	-	-	1	2
CO3	1	-	-	-	1	2
CO4	1	-	-	-	1	2
CO5	1	-	-	-	1	2
CO	1	-	-	-	1	2

AC22202	**நற்றமிழ் இலக்கியம்**	**L**	**T**	**P**	**C**
		2	**0**	**0**	**0**
UNIT I	**சங்க இலக்கியம்**				**6**
1. தமிழின் துவக்க நூல் தொல்காப்பியம் – எழுத்து, சொல், பொருள் 2. அகநானூறு (82) - இயற்கை இன்னிசை அரங்கம்					

3. குறிஞ்சிப் பாட்டின் மலர்க்காட்சி 4. புறநானூறு (95,195) - போரை நிறுத்திய ஔவையார்		
UNIT II	**அறநெறித் தமிழ்**	**6**
1. அறநெறி வகுத்த திருவள்ளுவர் - அறம் வலியுறுத்தல், அன்புடைமை, ஒப்புரவறிதல், ஈகை, புகழ் 2. பிற அறநூல்கள் - இலக்கிய மருந்து – ஏலாதி, சிறுபஞ்சமூலம், திரிகடுகம், ஆசாரக்கோவை (தூய்மையை வலியுறுத்தும் நூல்)		
UNIT III	**இரட்டைக் காப்பியங்கள்**	**6**
1. கண்ணகியின் புரட்சி - சிலப்பதிகார வழக்குரை காதை 2. சமூகசேவை இலக்கியம் மணிமேகலை - சிறைக்கோட்டம் அறக்கோட்டமாகிய காதை		
UNIT IV	**அருள்நெறித் தமிழ்**	**6**
1. சிறுபாணாற்றுப்படை - பாரி முல்லைக்குத் தேர் கொடுத்தது, பேகன் மயிலுக்குப் போர்வை கொடுத்தது, அதியமான் ஔவைக்கு நெல்லிக்கனி கொடுத்தது, அரசர் பண்புகள் 2. நற்றிணை - அன்னைக்குரிய புன்னை சிறப்பு 3. திருமந்திரம் (617, 618) - இயமம் நியமம் விதிகள் 4. தர்மச்சாலையை நிறுவிய வள்ளலார் 5. புறநானூறு - சிறுவனே வள்ளலானான் 6. அகநானூறு (4) - வண்டு நற்றிணை (11) - நண்டு கலித்தொகை (11) - யானை, புறா ஐந்திணை 50 (27) - மான் ஆகியவை பற்றிய செய்திகள்		
UNIT V	**நவீன தமிழ் இலக்கியம்**	**6**
1.உரைநடைத் தமிழ், - தமிழின் முதல் புதினம், - தமிழின் முதல் சிறுகதை, - கட்டுரை இலக்கியம், - பயண இலக்கியம், - நாடகம், 2.நாட்டு விடுதலை போராட்டமும் தமிழ் இலக்கியமும், 3. சமுதாய விடுதலையும் தமிழ் இலக்கியமும், 4.பெண் விடுதலையும் விளிம்பு நிலையினரின் மேம்பாட்டில் தமிழ் இலக்கியமும், 5.அறிவியல் தமிழ், 6.இணையத்தில் தமிழ், 7.சுற்றுச்சூழல் மேம்பாட்டில் தமிழ் இலக்கியம்.		
		TOTAL: 30 PERIODS

REFERENCES:

1	தமிழ் இணைய கல்விக்கழகம் (Tamil Virtual University)
2	தமிழ் விக்கிப்பீடியா (Tamil Wikipedia)
3	தர்மபுர ஆதீன வெளியீடு
4	வாழ்வியல் களஞ்சியம்
5	தமிழ்கலைக் களஞ்சியம் - தமிழ் வளர்ச்சித் துறை (thamilvalarchithurai.com)
6	அறிவியல் களஞ்சியம் - தமிழ்ப் பல்கலைக்கழகம், தஞ்சாவூர்